High Device Yield Carbon Nanotube NFETs for High-Performance Logic Applications

Davood Shahrjerdi, Aaron D. Franklin, Satoshi Oida, George S. Tulevski, Shu-Jen Han, James B. Hannon, and Wilfried Haensch

IBM Research, T. J. Watson Research Center, Yorktown Heights, NY, USA 10598
Email: davood@us.ibm.com

Abstract

We present the first analysis of device yield and material composition for several low work-function metal contacts to carbon nanotubes (CNT), including the first demonstration of high-performance n-channel field-effect transistors (NFET) from erbium (Er) and lanthanum (La). Our results indicate drastic improvement in NFET yield by appropriate metal selection and optimization of deposition conditions.

Introduction

One of the overriding challenges for developing a high-performance carbon nanotube device technology suitable for logic applications is to establish a manufacturable process for making reproducible NFETs. This calls for rigorous efforts beyond demonstrating the operation of a single device. While CNTs have been shown to provide p-channel FETs (PFET) with superb performance, achieving reproducible NFETs with comparable device performance and yield is still lacking. Although chemical doping [1] as well as electrostatic doping using high-k layers with high density of fixed charges overlaying the CNT channel [2] are shown to provide NFET device operation, these schemes do not appear to be viable options for highly integrated digital applications. Furthermore, recent reports have demonstrated the feasibility of yttrium (Y), scandium (Sc) and gadolinium (Gd) contacts to achieve excellent NFET operation [3-4], implying that the use of low work-function metals may provide a promising path for making high-performance CNT-NFETs. However, unlike the numerous reports investigating the role of various high work-function metals to realize high-performance CNT-PFETs with substantial device yield [5], until now there has been no such study for CNT-NFETs.

In this work, we present the first analysis of device yield for several low work-function metal contacts, including the first demonstration of high-performance CNT-NFETs from Er and La contacts. Device performance is further correlated with process development through extensive *in situ* material characterization. Our results indicate the ability to drastically improve the NFET yield by appropriate metal selection and optimization of deposition conditions.

Material Characterization

Table I lists several low work-function metals that are potentially suitable for making CNT-NFETs. In this work, we have examined Er and La metals –which are routinely used in mainstream silicon manufacturing– and compared the results with Y metal. The reason for selecting Y over Sc and Gd is that the previous reports show superior device performance with Y contacts to that of Sc and Gd contacts [3-4].

Table 1. Work-function comparison for some promising metal contacts for CNT-NFETs.

Metal	Work Function (eV)
Y	3.1
Gd	3.1
Er	3.0
La	3.5
Sc	3.5

Extensive material analysis using *in situ* x-ray photoelectron spectroscopy (XPS) was performed to correlate the electrical characteristics of the NFETs with the chemical properties of the low work-function metal contacts. Figure 1 illustrates the XPS spectra for the samples with 10nm thick Y and Er, monitored *in situ* under ultra high vacuum of 4×10^{-9} torr.

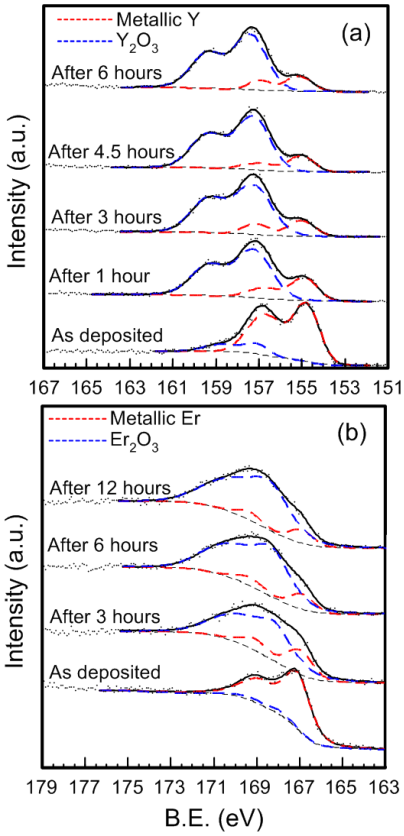

Figure 1: (a) Y *3d* and (b) Er *4d* XPS spectra of samples with 10nm Y and Er measured *in situ* as a function of time at 4×10^{-9}.

The oxide thickness was subsequently extracted from the fitted Gaussian curves to the XPS data and plotted as a function of time in Fig. 2, confirming the propensity of low work-function metals to rapidly oxidize, even under ultra high vacuum. Hence, the use of an effective scheme preventing the oxidation of metal contacts is crucial for realizing air-stable NFETs.

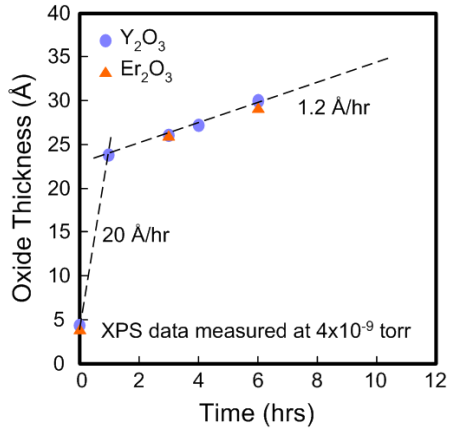

Figure 2: The growth dynamics of Y_2O_3 and Er_2O_3 extracted from the XPS spectra shown in Fig. 3, indicating initial fast oxidation of the metallic Y and Er. The oxide thickness saturates to ~3nm.

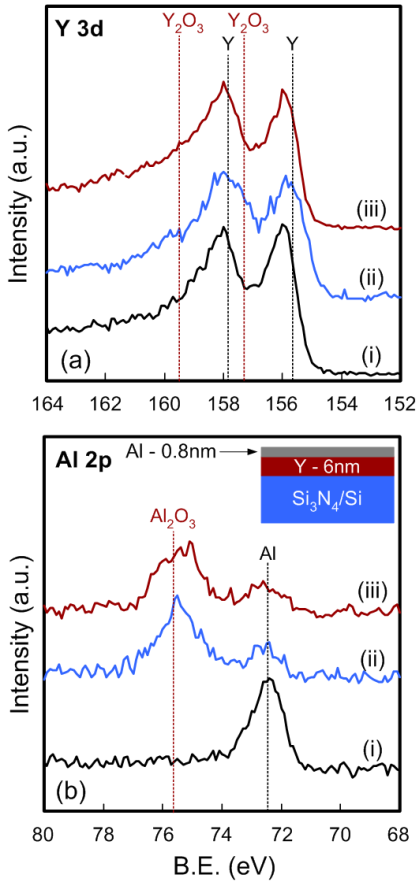

Figure 3: (a) Y *3d* and (b) Al *2p* XPS spectra of a sample with Y capped with Al measured (i) *in situ* immediately after deposition, (ii) after 3min exposure to air and (iii) after an additional 6 hrs wait in vacuum. The data indicates that a very thin layer of Al can effectively prevent oxidation of the Y metal.

The inset in Fig. 3b illustrates the XPS test structure, in which 6nm Y was capped *in situ* by 0.8nm aluminum (Al). It is notable that the Al capping layer was kept thin in this structure to allow the penetration of the x-ray into the underlying Y layer. It is evident from the XPS data (Fig. 3) that the use of a very thin Al capping layer can effectively prevent the oxidation of the low work-function contacts in air.

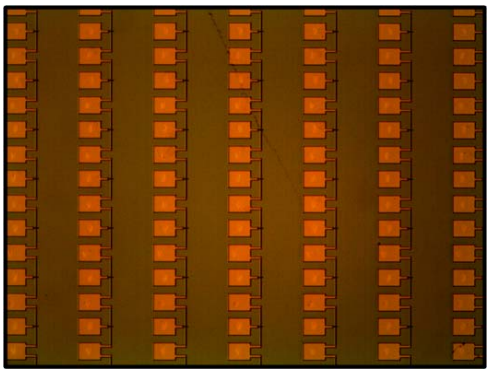

Figure 4: Optical image of a tested chip with 768 potential FETs.

Device Yield Study

To investigate the device yield from different low work-function metals, hundreds of devices were fabricated and tested using a semi-automated probestation. Figure 4 is an optical image of a tested chip. Each chip has 768 potential FETs, with a printed channel length of 300nm. Figure 5 (a) and (b) show the schematic illustration and the top-view SEM image of two NFETs, respectively. Devices in this study use a global back gate scheme with p^+ Si substrates capped with 10 nm thermal SiO_2 gate dielectric. Solution-processed CNTs were dispersed on the substrate prior to contact patterning by electron-beam lithography and metallization. The source-drain contacts were formed using a lift-off process. It should be noted that many of the CNTs may not cross the source/drain contacts due to the random distribution of the tubes on the surface. Additionally, the random orientation of the tubes may render the actual channel length for some devices to be greater than 300nm.

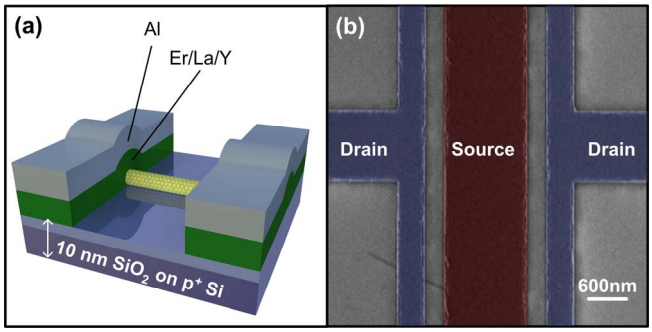

Figure 5: (a) Schematic illustration and (b) top-view SEM image of two CNT-NFETs. The low work-function metals were *in situ* capped by a thin layer of Al to prevent oxidation in air.

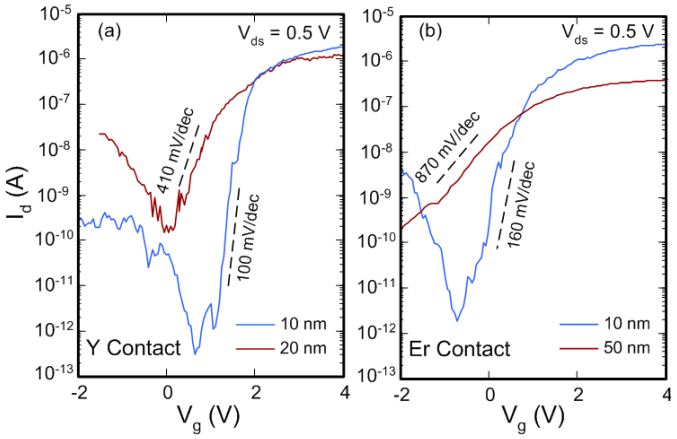

Figure 6: Representative I_d-V_g characteristics of CNT-NFETs illustrating the effect of (a) Er and (b) Y metal contact thickness deposited at 2.5-3 Å/min. The subthreshold characteristics of the devices with thicker low work-function metal considerably degrade due to a higher degree of Er or Y oxidation during the deposition.

As discussed in the previous section, low work-function metals are prone to oxidize even under ultra high vacuum conditions. It is therefore important to consider the impact that partial oxidation of the metal contacts during the evaporation process has on device performance. To investigate this effect, several chips were prepared with various Er and Y thicknesses evaporated at a slow deposition rate of ~2.5 Å/min. As can be seen in Fig. 6, performance degradation is more significant for the devices with thicker metal contacts—conceivably due to a higher degree of metal contact oxidation. It is also important to point out that the device yield on chips prepared at a slow deposition rate was extremely low–only ~5 or 6 devices exhibit NFET operation out of 768 potential FETs (note that the device yield is determined by comparing the number of functional devices on an NFET chip to that on PFET counterpart chips, discussed below). Hence, to diminish the adverse impact of metal contact oxidation, evaporations were performed at higher deposition rates, leading to significant improvement of the device characteristics. The representative transfer and output characteristics of a CNT-NFET with La contacts are shown in Fig. 7(a) and (b).

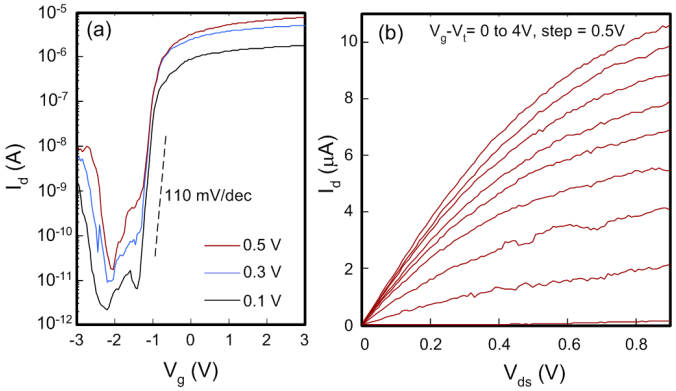

Figure 7: Representative (a) subthreshold and (b) output characteristics of a high-performance CNT-NFET with La contacts and a channel length of 300 nm.

In addition, using higher deposition rates was found to remarkably improve the device yield and performance of the CNT-NFETs. Our methodology for assessing device yield involves plotting the I_d-V_g curves measured at $|V_{ds}|$ = 0.5 V for a CNT-NFET chip and comparing the yield and performance to a CNT-PFET chip with Pd contacts, shown in Fig. 8. This comparison to PFET chips prepared from the same density CNT solution helps to rule out the chance for a yield discrepancy caused by a lack of CNT channels crossing potential contacts since the number of contacted CNTs should be fairly consistent

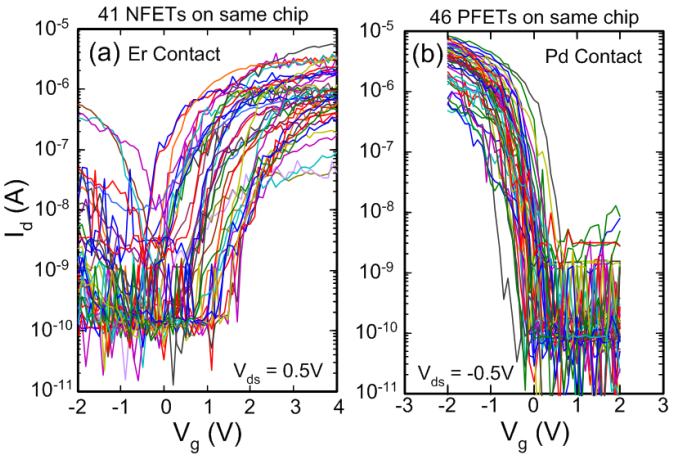

Figure 8: Comparison of I_d-V_g curves for two chips with (a) CNT-NFETs from Er contacts (high deposition rate) and (b) CNT-PFETs from Pd contacts, showing similar device yield.

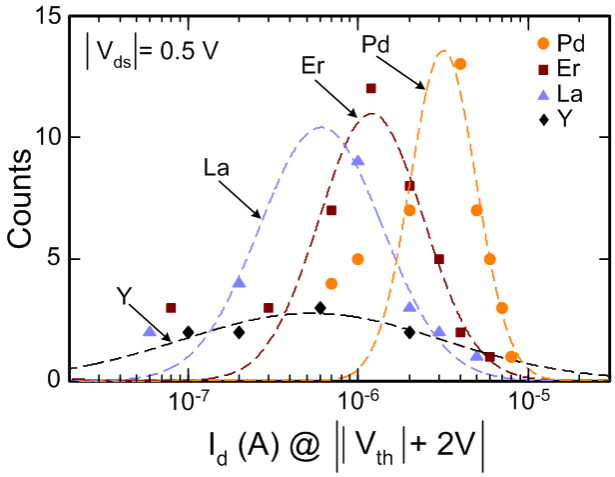

Figure 9: Comparison of on-current distributions from CNT-NFET chips with Er, La, and Y contacts versus a CNT-PFET chip with Pd contacts, extracted from I_d-V_g curves similar to Fig. 8. These distributions delineate the importance of material choice in improving device yield.

for all chips in this study. Therefore, a lower yield will be a direct result of poor metal contacts to nanotubes. Figure 9 delineates the on-current distribution data for Er, La, Y and Pd, extracted from similar I_d-V_g curves shown in Fig. 8. Comparing the various metals highlights the importance of the material choice in improving the yield of CNT-NFETs. The device yield for Er NFETs is rather comparable to the Pd PFETs, with the average on-current of the PFETs being slightly higher. However, it is important to note that the performance of our very best NFETs using Er and La is similar to that of the best

PFETs (Fig. 10). This result suggests that further optimization of the NFET process can reduce the remaining disparity in device performance between NFETs and PFETs.

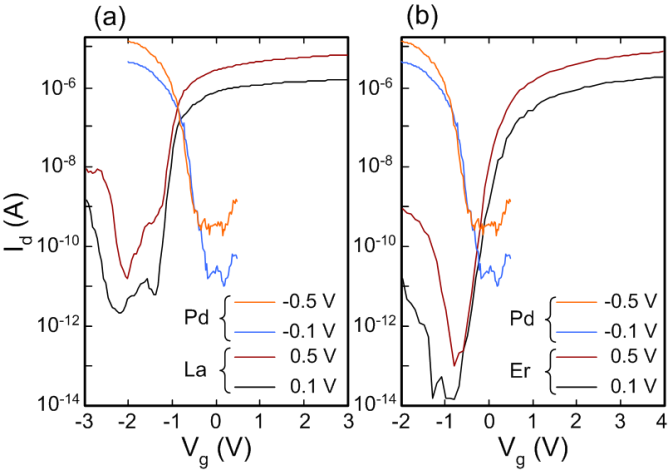

Figure 10: Transfer characteristics of representative 'best' devices with (a) Er and (b) La contacts overlaid on one of the best PFETs with Pd contacts, showing comparable performance.

It should be noted that the hysteresis window of our NFETs with no surface passivation is relatively large. This issue is one of the major device challenges for utilizing CNT-FETs in integrated digital applications. A. Franklin *et al.* has recently shown that the application of self-assembled hydrophobic monolayers, such as HMDS, for passivating bottom-gated PFETs dramatically suppresses the hysteresis window [6]. To investigate the benefits of similar passivation scheme in mitigating the hysteresis of NFETs, HMDS was deposited onto an NFET chip with Er contacts under ~1 torr at 150°C for 30 min. We observed that the application of the hydrophobic monolayer to the surface of NFETs effectively reduces the hysteresis window (Fig. 11).

Conclusion

Studying hundreds of CNT-NFETs from different low work-function metals has shown a substantial difference in device yield. Considerable improvements in device yield–comparable to CNT-PFETs–were observed when using Er contacts deposited with high deposition rates. High oxidation rates and sensitivity to deposition conditions are causes of the lower yield and large variation in performance of the NFETs. This work sets an important precedence for analyzing device yield when considering the validity of a certain metal contact for CNT-NFETs.

Acknowledgment

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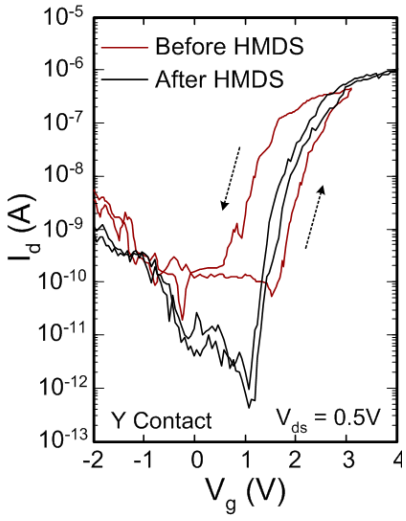

Figure 11: Reduction of hysteresis by employing a self-assembled monolayer passivation. Even though the device was tested in air, the n-branch is not suppressed and hysteresis is reduced.

Reference

[1] J. Chen, *et al.*, "Self-aligned Carbon Nanotube Transistors with Novel Chemical Doping", *IEDM 2004 Technical Digest*, p. 695, 2004.

[2] J. Zhang, *et al.*, " Change in Carrier Type in High-k Gate Carbon Nanotube Field-Effect Transistors by Fixed Charges", *Nanotechnology,* vol. 21, p. 165201, 2010.

[3] L. Ding, *et al.*, "Y-Contacted High-Performance n-Type Single-Walled Carbon Nanotube Field-Effect Transistors: Scaling and Comparison with Sc-Contacted Devices", *Nano Lett.*, vol. 9, p. 4209, 2009.

[4] C. Wang, *et al.*, "Metal Contact Engineering and Registration-Free Fabrication of Complementary Metal-Oxide Semiconductor Integrated Circuits Using Aligned Carbon Nanotubes", *ACS Nano*, vol. 5, p. 1147, 2011.

[5] Y. –C. Tseng, *et al.*, "Effect of Diameter Variation in a Large Set of Carbon Nanotube Transistors", *Nano Lett.*, vol. 6, p. 1364, 2006.

[6] A. Franklin, *et al.,* "Variability in Carbon Nanotube Transistors—Improving Device-to-Device Consistency", (in review).