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High-density integration of carbon nanotubes via chemical self-assembly

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Carbon nanotubes have potential in the development of high-speed and power-efficient logic applications[1–7]. However, for such technologies to be viable, a high density of semiconducting nanotubes must be placed at precise locations on a substrate. Here, we show that ion-exchange chemistry can be used to fabricate arrays of individually positioned carbon nanotubes with a density as high as 1×10^9 cm^{-2}—two orders of magnitude higher than previous reports[8,9]. With this approach, we assembled a high density of carbon-nanotube transistors in a conventional semiconductor fabrication line and then electrically tested more than 10,000 devices in a single chip. The ability to characterize such large distributions of nanotube devices is crucial for analysing transistor performance, yield and semiconducting nanotube purity.

The precise placement of carbon nanotubes on a substrate typically involves one of three techniques: the direct growth of nanotubes on a substrate[10,11], the transfer of nanotubes from a 'growth' substrate to a device substrate[5,6], or the deposition of nanotubes from solution onto a device substrate[8,9,12–18]. Because nanotubes can be metallic or semiconducting, a further consideration for high-performance digital logic is the degree to which metallic nanotubes can be eliminated. Although approaches for enriching substrate-supported semiconducting nanotubes during or after synthesis have been demonstrated[19,20], currently the most effective techniques involve processing the nanotubes in solution[21].

One promising approach for placing solution-based nanotubes is to selectively position them on a specific substrate by chemically functionalizing the nanotubes or the substrate[14–18]. This typically involves using a patterned surface (such as SiO_2/HfO_2) such that nanotubes deposited from solution adhere only to one part of the pattern (the HfO_2, for example). Key metrics for determining the efficacy of the deposition are the density of individually placed nanotubes, which must exceed 1×10^{10} cm^{-2}, with a pitch smaller than 10 nm for high-performance logic[6,7], and the selectivity, which is the degree to which adsorption takes place only on the pattern of interest. In general, however, solution-based approaches that result in high density exhibit poor selectivity[14,16], and those that offer high selectivity have low density[17,18].

We have developed a selective placement method based on ion exchange between a functional surface monolayer and surfactant-wrapped carbon nanotubes in aqueous solution. Strong electrostatic interaction between the surface monolayer and the nanotube surfactant leads to the placement of individual nanotubes with excellent selectivity and a density of 1×10^9 cm^{-2}. Furthermore, the approach is compatible with the most efficient solution-based separation schemes[21], allowing wafer-scale integration using highly purified carbon nanotubes.

Our nanotube placement using an ion-exchange technique is illustrated in Fig. 1a. The surface monolayer is formed from 4-(*N*-hydroxycarboxamido)-1-methylpyridinium iodide (NMPI) molecules, which were synthesized from commercially available methyl isonicotinate (see Methods). The monolayer contains a hydroxamic acid end group that is known to self-assemble on metal oxide surfaces, but not on SiO_2 (refs 17,18,22). We selectively self-assembled NMPI on HfO_2 regions of a patterned SiO_2/HfO_2 surface. The functionalized surface was then placed in an aqueous solution of carbon nanotubes. Solubility of the nanotubes was achieved using an anionic surfactant (sodium dodecyl sulphate, SDS). Excess surfactant in the solution was removed by dialysis. The anion of NMPI (that is, iodide) is exchanged with the anionic surfactant wrapped around the nanotubes, leading to a strong coulombic attraction between the negatively charged surfactant and the positively charged monolayer. In this process, the iodide of the monolayer and the sodium ion of the surfactant are removed as sodium iodide, which is dissolved into the solution. The exchange mechanism was verified using X-ray photoelectron spectroscopy (XPS) measurements made before and after exposure of the monolayer to the surfactant (Supplementary Fig. S1).

To assess the selectivity and density of this placement technique, arrays of long, narrow HfO_2 trenches were fabricated on a SiO_2 substrate. Carbon nanotubes were selectively deposited on HfO_2 regions coated by NMPI (see Methods). Scanning electron microscopy (SEM) and atomic force microscopy (AFM) images recorded after nanotube deposition are shown in Fig. 1b–d. On the larger, open HfO_2 areas (Fig. 1b), the deposited nanotubes are well dispersed and form monolayers with extremely high density and excellent selectivity. High density and selectivity are maintained even in the narrower trenches (200 nm, Fig. 1c,d).

When positioning nanotubes on a substrate, it is critical to be able to control their alignment in addition to their location. Angular misalignment leads to a corresponding variation in the nanotube channel and contact lengths of transistors fabricated with the nanotubes, resulting in unacceptable variation in device performance. Achieving high selectivity in the present approach not only ensures accurate location positioning, but also promotes alignment of the nanotubes along a trench. Figure 2a shows how the alignment improves as the trench width (W_{tr}) is reduced. By reducing W_{tr} to 70 nm, the angular variation of the nanotubes relative to the trench axis is reduced to less than $\pm 30^\circ$. Figure 2b shows nanotubes selectively placed in an array of 70-nm-wide HfO_2 trenches with 200 nm pitch.

While placement in long, narrow lines is useful for characterizing alignment and density, device applications require precise confinement of nanotubes in both dimensions, that is, on narrow and short lines. Figure 2c presents an SEM image of nanotubes deposited onto an array of short and narrow trenches with 200 nm pitch in the *x* direction and 500 nm pitch in the *y* direction, corresponding to a density of 1×10^9 sites cm^{-2}. This density represents an

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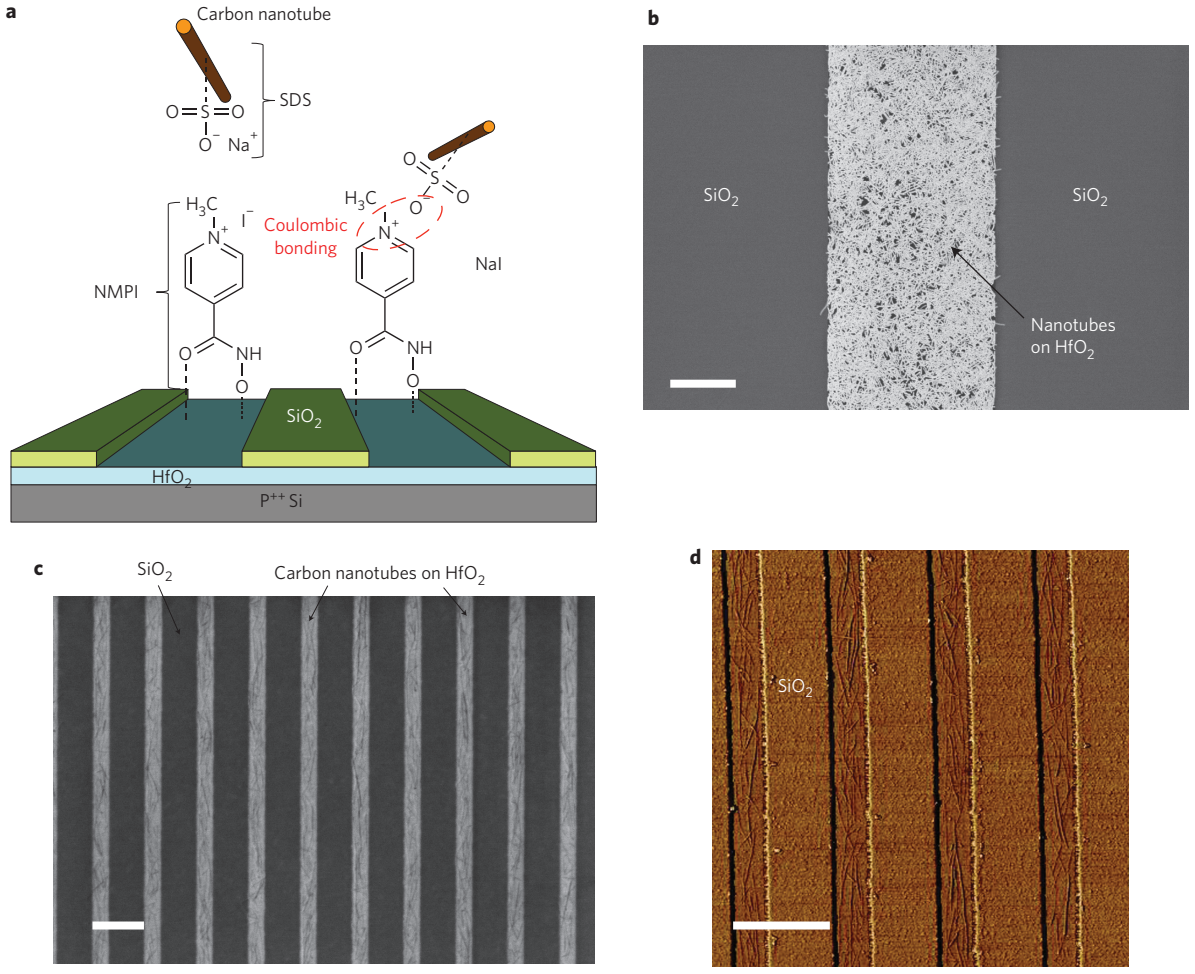

Figure 1 | Selective placement of carbon nanotubes by an ion-exchange process. a, Schematic of nanotube placement on the surface monolayer, which is selectively coated on the HfO_2 regions. The iodine ion in the end group of the NMPI monolayer is exchanged by the negatively charged SDS surfactant wrapping the nanotubes; Na^+ in SDS and I^- in NMPI are dissolved into solution as a sodium iodide. The thickness of SiO_2 is 10 nm and the width of the HfO_2 trenches varies from 70 nm to 200 nm. The P^{++} Si layer is a highly doped p-type Si substrate. **b**, SEM image of nanotubes deposited on an open HfO_2 area, showing extremely high density and excellent selectivity (scale bar, 2 μm). **c**,**d**, SEM image (**c**) and AFM (phase) image (**d**) of the nanotubes selectively deposited on an array of 200-nm-wide HfO_2 trenches. Good density and selectivity are maintained on these narrower trenches. Scale bars are 500 nm.

improvement of two orders of magnitude over previously reported results obtained using microcontact printing[8], dielectrophoresis[9] or a scanning probe[12]. As determined from more than 350 trench images, the placement yield was ~90% (that is, 90% of the trenches contained at least one nanotube). However, a more comprehensive yield can be evaluated by measuring the electrical properties (for example, resistance) of transistors fabricated on the placed nanotubes; for the transistor to work, the nanotube must be properly positioned in the trench so as to span the defined source and drain electrodes.

This ability to accurately place individual, aligned nanotubes at a high density enables the fabrication of a large number of nanotube transistors on a single chip. Using the placement method, we fabricated thousands of transistors with a channel length (spacing between source and drain contacts) of 100 nm. As estimated from SEM images of the channel regions, the average number of nanotubes per channel was dependent on the trench dimensions and the concentration of nanotubes in the deposition solution; narrower trenches and more diluted nanotube solutions resulted in a larger fraction of single-nanotube transistors (up to ~78%; Supplementary Fig. S3). Direct numerical simulation of the measured distributions of nanotubes per channel suggests that the probability of a nanotube from solution adhering in an empty trench is roughly three times higher than that of adhering in an occupied trench (Supplementary Fig. S4). This propensity to form single-nanotube trenches is an important advantage of this approach.

Figure 3a presents images of the channel regions of an array of nanotube transistors with a device pitch of 300 nm—an order of magnitude smaller than previous reports (~5 μm)[9]. Each transistor contained one trench of width 100, 150 or 200 nm and length 1 μm. Because the nanotube transistors were designed and fabricated using a conventional semiconductor fabrication facility, characterization of the devices was compatible with high-volume electrical characterization tools, enabling rapid testing of thousands of devices. Plots of drain current (I_D) versus gate voltage (V_G) from a subset of devices on a chip (~300 devices) are shown in Fig. 3b. The curves provide valuable insight into the variation that exists in the nanotube transistors, in addition to the population of devices that contained a metallic nanotube. A device yield of >90% was obtained with 150 nm and 200 nm trench widths; as the trench width decreases, the yield of semiconducting devices increases, which is attributed to the yield of single-nanotube devices increasing (Supplementary Fig. S5). The highest device yield was achieved after optimizing the surface-cleaning step that takes place before deposition of the NMPI monolayer; in other words, the density of NMPI, and thus nanotube density, is dependent on the surface cleanliness.

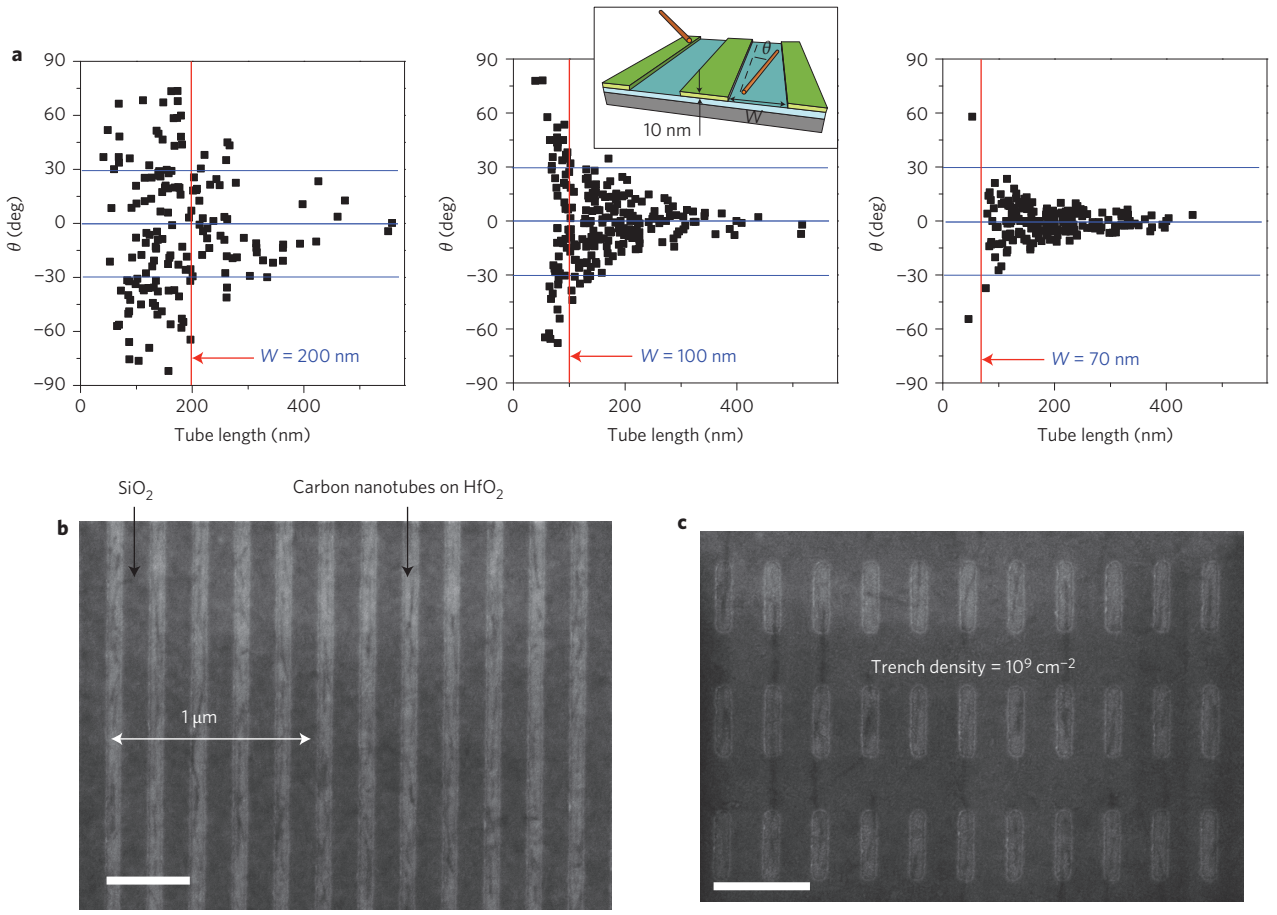

Figure 2 | High density of individually positioned carbon nanotubes. a, Plots of angular alignment of individual nanotubes versus length of the nanotube for trenches of three different widths ($W = 200$ nm, 100 nm, 70 nm). Inset: schematic showing how the angular alignment θ is defined (0° is perfect alignment in a trench). By reducing the trench width to 70 nm, the angular variation was reduced from ±75° to less than ±30°. **b**, SEM image of nanotubes selectively placed and well-aligned in an array of 70-nm-wide HfO_2 trenches with a 200 nm pitch (scale bar, 400 nm). **c**, SEM image of nanotubes selectively placed in an array of short and narrow trenches with a 200 nm pitch in the *x* direction and 500 nm pitch in the *y* direction, corresponding to a density of 10^9 sites cm^{-2} (scale bar, 400 nm). This demonstrates precise placement in two dimensions (rather than just one dimension with the long trenches in **b**). As determined from more than 350 trench images, ~90% of the trenches contain at least one nanotube.

For fast assessment of the key device parameters from a large number of devices, the measured characteristics for each transistor were modelled by fitting the measured I_D–V_G curves to a parametric function (see Methods). Representative curve fits are shown in Fig. 3c. Figure 3d shows the distributions of the threshold voltage (V_T) and inverse subthreshold slope (SS) extracted from 7,066 semiconducting devices. These devices were selected from about 12,000 connected nanotube devices by excluding devices that did not exhibit current levels expected for the transistor dimensions, and so on (such devices typically contained a metallic nanotube or an extremely short contacted length, leading to high contact resistance and low current[5]). In this analysis, V_T was defined as the gate voltage corresponding to a drain current of 3 nA. The average on-state drain current (I_{on}), measured at $V_G = V_T - 1.5$ V and $V_{DS} = -0.5$ V, was 1.33 μA. These results show that the performance of devices fabricated using the chemical assembly is comparable to that produced by the deposition of nanotubes from solution that did not undergo the same chemical treatments[23–25]. Annealing the wafer after nanotube deposition to remove the NMPI monolayer is crucial to maintaining this good electrical performance (Supplementary Fig. S6).

Before this study, device metrics for nanotube transistors, such as I_{on}, V_T, SS and the purity of semiconducting devices, were typically evaluated from, at most, a few hundred devices[23–27]. However, to realistically consider carbon-nanotube transistors for a technology, the distribution in performance across tens of thousands of devices must be statistically analysed and optimized. One key example comprises the accurate measurement of the fraction of metallic nanotubes in a solution. Metallic nanotubes lead to transistor 'shorts', and must be largely eliminated. A competitive carbon-nanotube logic technology requires an extremely high purity of semiconducting devices, with a metallic fraction less than at least 1×10^{-4}. Measuring this level of purity in solution has not proven possible, leaving large-scale device fabrication and testing as the only viable method. Our new ion-exchange placement approach provides a platform for such testing to be realized. The capability of measuring the device parameter distributions from a large number of nanotube transistors will also be critical in developing robust wafer-scale processes for carbon-nanotube integrated circuits.

In summary, we have demonstrated a new ion-exchange surface chemistry approach for the placement of individual carbon nanotubes with a density of 1×10^9 cm^{-2}. The method combines excellent selectivity with nanotube alignment at a high density to enable the formation of single-nanotube devices. The compatibility of this approach with existing semiconductor technology was shown by fabricating tens of thousands of nanotube transistors within a conventional fabrication facility. Electrical testing shows that the performance of nanotube devices is not significantly degraded by the deposition chemistry. This new placement technique is readily

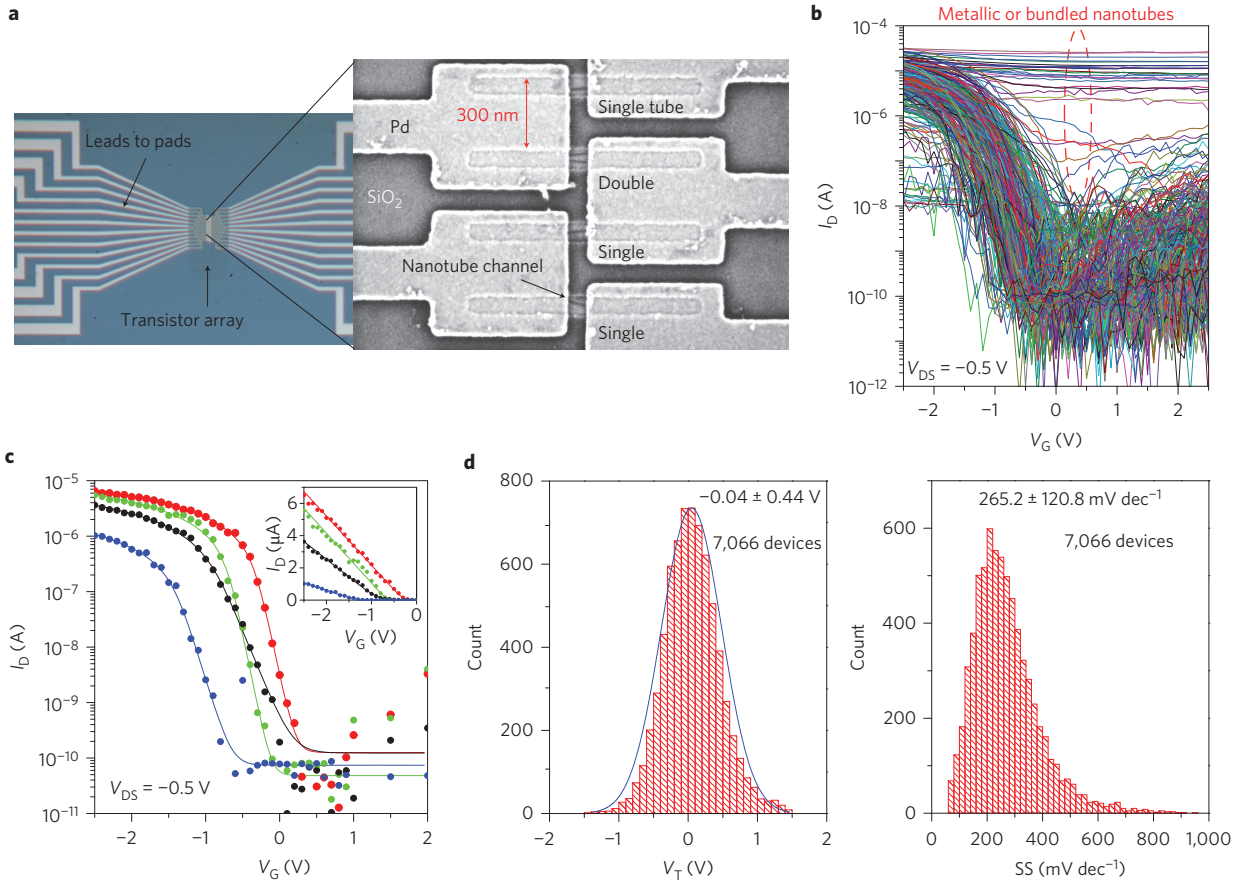

Figure 3 | Demonstration of high-density carbon nanotube transistors (CNTs). a, Optical (left) and SEM (right) images of nanotube transistor arrays with a pitch of 300 nm. Source and drain contacts for the devices in the array are connected by metal leads and pads for electrical testing in a semi-automated probe station. The achievable device density estimated from the device pitch and trench dimension is $>1 \times 10^8$ transistors cm^{-2}. (Contrast and brightness in the vicinity of nanotubes have been adjusted to make them more visible.) **b**, Subthreshold characteristics (log(I_D)-V_G curves) from a subset (310 devices) of total devices on a chip. The yield of electrically connected devices is larger than 90% (evaluated from measurement of 3,312 devices). **c**, Four representative I_D-V_G data (dots) from the large sets of devices measured in a semi-automated probe station and curves fitted using a parametric function (solid lines). Device parameters (V_T, I_{on}, SS) can be assessed from the fitted curves. Inset: plots in a linear scale. **d**, Distribution of threshold voltages (left) and inverse SS (right) extracted from measurements of 7,066 semiconducting nanotube transistors on a single chip. The ability to analyse key performance metrics from such a large number of devices provides valuable information regarding variability and yield and is a critical advance for a carbon-nanotube transistor technology.

implemented, involving common chemicals and processes, and provides a platform for future nanotube transistor experimental studies. Furthermore, these results show that nanotube placement via chemical self-assembly is a promising approach for developing a viable carbon-nanotube logic technology compatible with existing semiconductor fabrication.

Methods

Synthesis of NMPI molecules. The surface monolayer was formed from NMPI molecules, and was synthesized in two steps from the commercially available methyl isonicotinate. Methyl isonicotinate was converted to its corresponding hydroxamic acid, 4-(*N*-hydroxycarboxamido)pyridine, using a previously described procedure in ref. 28. Methyl iodide (10 g) was added to a solution of 4-(*N*-hydroxycarboxamido)pyridine (5.14 g, 0.03 mol) in 200 ml of methanol, and the mixture was stirred at room temperature for 3 days. The precipitate was filtered and washed with methanol and dried. Crystallization from 9:1 ethanol–water afforded the analytically pure pyridinium compound NMPI as light yellow crystals (7.35 g, 84%). ^{1}H NMR (DMSO-d6), δ; 4.38 (s, 3H), 8.3 (d, $j = 6$ Hz, 2H), 9.1 (broad d, $j = 6$Hz, 2H).

Purification of single-walled carbon nanotubes. A 1 g ml^{-1} solution of carbon nanotubes (Hanhwa Nanotech) in 1% aqueous SDS (Sigma Aldrich) was prepared via horn sonication (99%, 1 s pulse, 20 min). The solution was then purified using a step-gradient ultracentrifugation process. For the purification, 6 ml of 1% SDS in 45% iodixdinol (Sigma Aldrich) solution was prepared and layered below 6 ml of the nanotube solution in a 12 ml centrifuge tube. The layered solution was then centrifuged for 15 h at 41,000 r.p.m. using a Beckman Coulter Optima L-100 XP ultracentrifuge equipped with a swinging bucket-type rotor. The purified nanotube solution sedimented at the interface of the two layers while the graphitic impurities and large bundles settled to the bottom of the centrifuge tube. The purified nanotube solution was then removed via pipette and diluted 1:1 with 1% aqueous SDS solution before loading on the column. It is important to note that this step-gradient centrifugation step is only used to remove the graphitic impurities and concentrate the solution (very effective) and does not sort the nanotubes in any fashion. A chromatography step was then performed to isolate the semiconducting nanotubes.

Isolation and dialysis of semiconducting-enriched carbon-nanotube solution. The semiconducting nanotubes were separated from the purified nanotube solution by means of column chromatography, which was modified from a previously reported method described in ref. 29. A column was prepared by loading a 25-mm-diameter glass chromatography column with a Sephacryl-200 slurry (Sigma Aldrich). The column was flushed with 1% wt/vol SDS solution several times. The nanotube solution was then added to the column and allowed to pass through the column using a small positive nitrogen gas pressure. Once the solution was fully inserted into the column, more 1% SDS solution was added and was continually added until all of the nanotubes (now separated) passed through the column. Initially, a blue fraction (metallic) passed through, followed by a red band (semiconducting). Fractions of the solution were collected in small glass vials and characterized using a UV–vis–NIR absorption spectrometer (Perkin Elmer Lambda 950). Excess SDS in the solution was removed via dialysis, with the concentrated nanotube solution syringed into a dialysis cartridge and placed in 1 l of deionized water and changed daily for four days.

Fabrication of carbon-nanotube transistors. To assemble the carbon nanotubes, HfO_2 trenches were fabricated by patterning SiO_2 on HfO_2-coated substrates. First,

10 nm HfO_2 was deposited on a highly doped p-type silicon substrate via chemical vapour deposition (precursor, hafnium-tetra-tert-butoxide $Hf(C_4H_9O)_4$; carrier gas, O_2; working pressure/temperature, 0.3 torr/500 °C) and treated by a rapid thermal annealing at 700 °C in a N_2 atmosphere. Trench patterns were defined by electron-beam lithography (in PMMA), deposition of 5 or 10 nm of SiO_2 by electron-beam evaporation with a deposition rate of 0.2 nm s^{-1}, and liftoff in acetone. Note that the role of the evaporated SiO_2 layer was to prohibit the deposition of nanotubes so as to achieve the demonstrated excellent selectivity, and the layer was not included in the gate dielectric of final devices. Before self-assembly of the NMPI monolayer, the substrate was cleaned by oxygen plasma at 300 mtorr for 5 min. The NMPI monolayer was then assembled on the patterned surface by placing the substrate in a 3.5 mM solution of NMPI (3:1 ethanol/water) for 1 h. The surface was then rinsed with ethanol. The substrate was then placed horizontally with its surface facing upwards in the dialysed nanotube solution for 1 h, without an agitation. After nanotube deposition, the substrate was rinsed with flowing deionized water for 30 s and subsequently in a sonication bath with deionized water for 1 min. The substrate was then annealed at 450 °C under Ar/H_2 for 5 min to drive off the monolayer and eliminate its effects on device performance. Source and drain electrodes (Ti/Pd/Au = 0.5/20/20 nm) were patterned on the nanotubes via electron-beam lithography with a channel length of 100 nm. The highly doped silicon substrate was used as a backgate. In the deposition process, an effective cleaning process was critical to achieve a high density of placed nanotubes. The majority of the electrical characterization for large device sets in this work was performed on wafers that had been cleaned with a 700 °C anneal in oxygen before NMPI deposition. However, this process only provided a device yield of ~50%. A subsequent wafer that was subject to the oxygen plasma cleaning step resulted in the ~90% yield.

Fitting measured V_G–I_D curves. The measured data from large sets of devices were automatically analysed by fitting each measured curve to the expression

$$I_D(V_G) = I_{off} + \alpha \ln(1+z) + \beta \frac{z}{1+z}$$

where $z = \exp[(V_T - V_G)/SS]$. The five fitting parameters are V_T, I_{off}, SS, α and β. I_{off} is the off-state drain current defined as $I_D(V_T + 1\ V)$. This strictly empirical fitting function includes all the necessary features to allow a good fit and analysis: a small off-state current, a voltage threshold and an exponential rise near the threshold.

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Author contributions

H.P., A.A., G.S.T. and S.H. developed the carbon nanotube placement method. H.P., S.H. and A.D.F. fabricated and characterized the nanotube transistors. J.B.H., J.T. and W.H. developed the model and software for rapid assessment of the large sets of measured data. All authors contributed to discussing the results and writing manuscript.

Additional information

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Competing financial interests

The authors declare no competing financial interests.