NANO LETTERS

LETTER

pubs.acs.org/NanoLett

High-Frequency Graphene Voltage Amplifier

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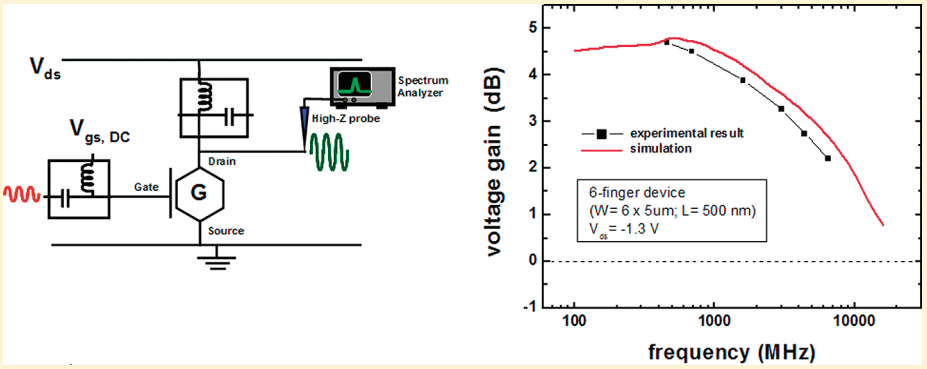
ABSTRACT:



While graphene transistors have proven capable of delivering gigahertz-range cutoff frequencies, applying the devices to RF circuits has been largely hindered by the lack of current saturation in the zero band gap graphene. Herein, the first high-frequency voltage amplifier is demonstrated using large-area chemical vapor deposition grown graphene. The graphene field-effect transistor (GFET) has a 6-finger gate design with gate length of 500 nm. The graphene common-source amplifier exhibits ~5 dB low frequency gain with the 3 dB bandwidth greater than 6 GHz. This first AC voltage gain demonstration of a GFET is attributed to the clear current saturation in the device, which is enabled by an ultrathin gate dielectric (4 nm HfO_2) of the embedded gate structures. The device also shows extrinsic transconductance of 1.2 mS/μm at 1 V drain bias, the highest for graphene FETs using large-scale graphene reported to date.

KEYWORDS: Graphene, amplifier, circuit, voltage gain, current saturation

Because of the remarkable transport properties of graphene,[1−4] there is tremendous interest in using this two-dimensional (2D) material as a channel material for future radio frequency (RF) transistors. Recently, much progress has been made in graphene RF technology with focus on high unity-current gain cutoff frequencies (f_T) of graphene field-effect transistors (GFETs).[5−7] These high f_T numbers result directly from graphene's high mobility; however, since the drain current does not saturate in these devices, they exhibit limited power gain, lack voltage gain, and hence are not useful for practical RF circuit applications. Although voltage gain has been demonstrated using double-gated bilayer graphene flakes (to open the band gap), the device had to be cooled to 77 K in order to observe gain.[8] Several recently reported graphene-based circuits measured at room temperature were far from obtaining any gain and could only operate in some specialized function based on graphene's ambipolar property or nonsaturated behavior.[9−11] An important next step is the demonstration of more generalized circuit functions, such as signal amplification, that are required in most analog circuits.

This Letter demonstrates the first high-frequency graphene voltage amplifier. The amplifier shows ~5 dB low frequency gain with the 3 dB bandwidth greater than 6 GHz. Chemical vapor deposition (CVD) grown graphene films are used in these GFETs.[12] An embedded gate structure with an very thin gate oxide leads to clear current saturation and low output conductance (g_{ds}, as low as 0.1 mS/μm) that enables high-frequency voltage gain. The amplifier presented here, consisting of a graphene FET and a high load impedance, was also simulated in a RF circuit simulator, showing that the device is capable of voltage amplification for frequencies exceeding 15 GHz. This demonstration of a GFET operating as an amplifier is evidence of the potential for this material to enable realistic, advanced RF circuitry.

The majority of fundamental FET-based analog circuits require devices with drain current saturation or, equivalently, high output resistance. Unlike semiconductor FETs, which saturate due to an energy band gap that leads to channel pinch-off, graphene is gapless and thus will not saturate by conventional means. Drain current saturation in graphene FETs can occur by a different mechanism when very thin gate dielectrics are used. Previous work has shown that the shift of the minimum conductivity point (V_{Dirac}) in GFETs with good gate control (i.e., no short channel effect) should be equal to half of the applied drain bias (V_{ds}).[13] With a very thin gate dielectric, the required gate bias (V_{gs}) for typical device operation becomes comparable to

Received: May 17, 2011
Revised: July 20, 2011
Published: August 01, 2011

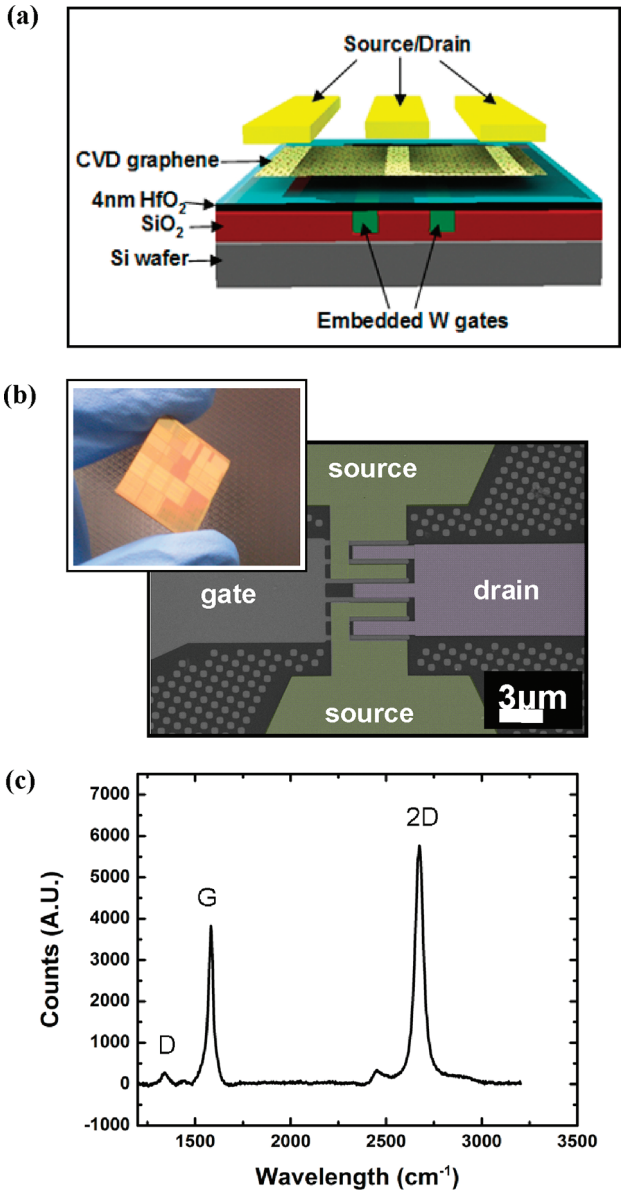


Figure 1. (a) Schematic of the embedded gate structure. CVD graphene pieces were transferred onto an 8 in. wafer with prepatterned metal gates covered by a high quality high-κ dielectric. (b) Scanning electron microscope image of a 6-finger device with 500 nm gate length. Inset shows photograph of a finished die (with graphene piece) fabricated in a Si-fab. (c) Raman spectra of CVD-grown graphene.

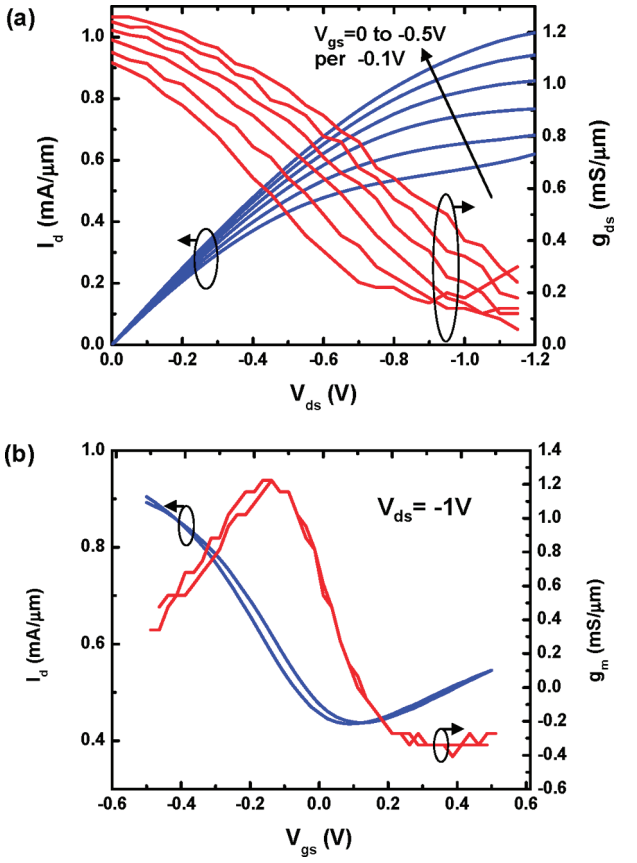


Figure 2. (a) Output characteristics from a 6-finger (5 μm × 6), 500 nm channel device. Clear drain current saturation is observed at relatively low bias conditions. (b) Transfer curve (I_d−V_{gs}) at V_{ds} = −1 V from the same device.

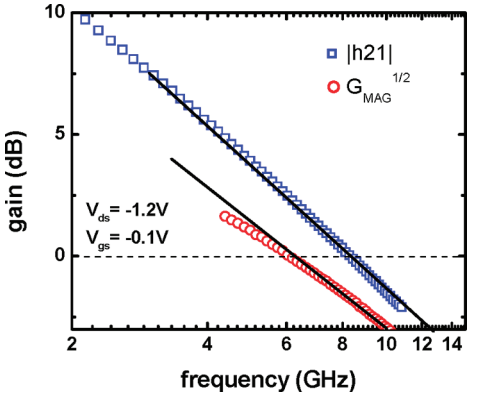


Figure 3. Measured power gain $(G_{MAG})^{1/2}$ and current gain |h21| as a function of frequency for the same 6-finger (5 μm × 6), 500 nm channel device. f_{MAX} and f_T are the frequency at which power gain and current gain becomes unity (0 dB), respectively.

V_{ds}, and I_d−V_{gs} curves move closer to each other with increasing drain bias. This V_{Dirac} shifting translates into a clear drain current saturation. However, depositing high-quality, thin gate dielectrics on this inert material is quite challenging.[14−16]

To obtain current saturation in submicrometer graphene FETs, an embedded metal gate structure was developed. The device, which was fabricated on 200 mm wafers with conventional silicon process technology, is illustrated in Figure 1a. In this structure, high-resistivity Si wafers with 1 μm thick thermal SiO_2 were used as a starting material. High-power reactive ion etching was used to form 200 nm deep trenches in the SiO_2, and 400 nm W was deposited. The wafer was then chemical−mechanical polished to planarize the W and complete the embedded gates.[17] An ultrathin high-κ dielectric (4 nm of HfO_2) with equivalent oxide thickness (EOT) of 1.75 nm was deposited and single-layer CVD-grown graphene films of 2 cm × 2 cm were transferred onto the substrate. The CVD growth and subsequent transfer of graphene followed processes reported in ref 12. Electron beam evaporation of 30 nm Pd/30 nm Au followed by a lift-off process

dx.doi.org/10.1021/nl2016637 |Nano Lett. 2011, 11, 3690–3693

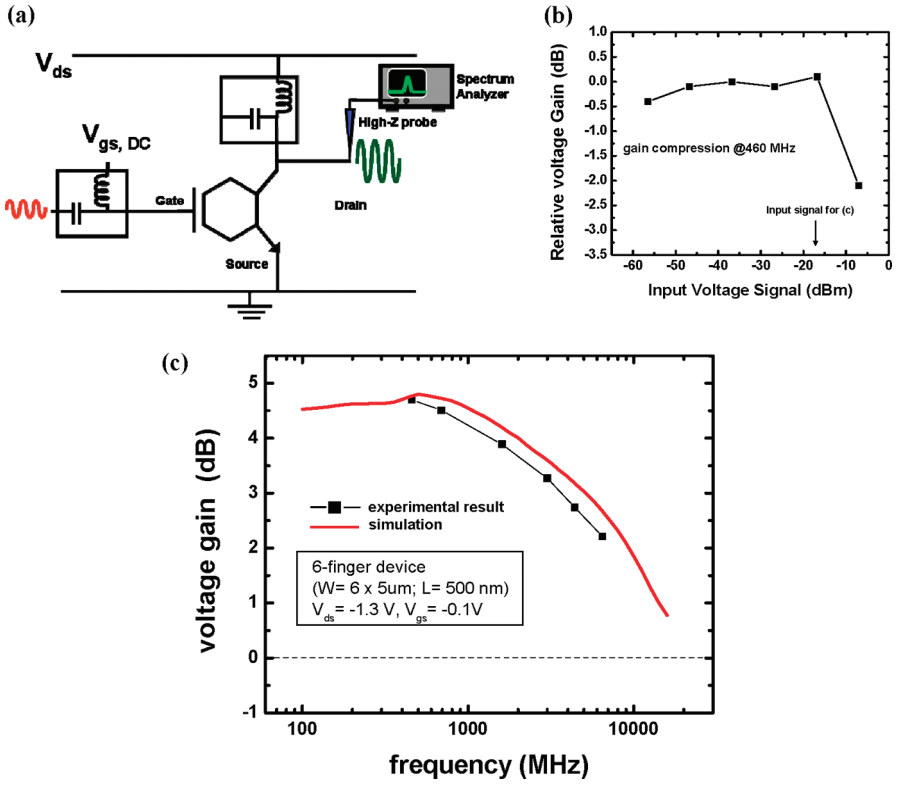


Figure 4. (a) Schematic of the graphene amplifier measurement technique. (b) Relative voltage gain as a function of input signal level. (c) Measured and simulated frequency response of the amplifier's voltage gain with the input signal level of −17 dBm.

was used to define source/drain electrodes. This embedded gate structure eliminates seed layers typically used in conventional top-gate schemes and largely improves the stability and manufacturability of GFETs. Because the graphene film is transferred onto prefinished gate stacks, different gate dielectrics, including those with higher phonon energy, can be potentially incorporated into GFETs more easily to further improve the device performance.[18] Figure 1b shows a scanning electron microscope (SEM) image of a 6 gate-finger device and the inset shows a photograph of the finished die. Raman spectroscopy was performed to confirm that the graphene was single layer, and the resulting spectrum is shown in Figure 1c. The presence of a sharp and intense 2D peak indicates that the graphene is monolayer, while the high G/D ratio indicates the good graphene quality.

Figure 2a shows the drain current (I_d) as a function of drain voltage (V_{ds}) at various gate-source bias (V_{gs}) conditions along with the corresponding output conductance, g_{ds}, defined as dI_d/dV_{ds}, from a graphene FET having a device width of 5 μm × 6 (6 fingers) and gate length of 500 nm. Drain current saturation is seen at relatively low V_{ds} (<−1 V) yielding a desirably low g_{ds}. The transfer curve in Figure 2b shows I_d as a function of gate voltage at a drain bias of −1 V. Minimum conductivity occurs well within the operating bias range (±0.5 V) and the device exhibits clear ambipolar behavior. A peak extrinsic transconductance, g_m (defined as dI_d/dV_{gs}), of ∼1.2 mS/μm is exhibited, which is the highest g_m for GFETs using large-scale graphene and among the highest reported for exfoliated graphene FETs.[6] This results from the very thin gate dielectric, which is made possible by the embedded gate structure. The minimal hysteresis in Figure 2b also demonstrates the high quality of the gate dielectric. Figure 3 shows RF characteristics of the graphene FET from s-parameter measurements. The extrinsic f_T and f_{MAX} (without de-embedding of parasitic capacitances and resistances) of a typical device were measured to be 8.2 and 6.2 GHz, respectively. The slight deviation from $1/f$ trend is attributed to the effect of parasitic capacitance. Note that f_{MAX} is about 80% of f_T as a result of the current saturation and 6-finger design, which reduces the gate resistance, of the devices.

However, neither f_T nor f_{MAX} guarantee that a device will be able to amplify when loaded by a practical impedance value. f_T is a figure of merit to evaluate fundamental transistor signal propagation delay. It is a measure of the short-circuit current gain of the device obtained from a transformation of s-parameters measured in 50 ohm measurement system. Since the output of the device is short-circuited, cutoff frequency does not assess the gain of a device which has a realistic, nonzero, load. For this, several power gain figures of merit, known generally as f_{MAX}, have been derived. These power-gain figures of merit assume that the source and load impedances presented to the device at a given frequency can be set to specific values that would allow for maximum power transfer. However, these impedances may not be realizable in a practical circuit. For example, nonsaturating devices with low output impedance may be able to deliver current (and power) gain only when loaded by an impedance that is close to a short circuit. Given that the input impedance of most transistors (including graphene FETs) is high, multistage amplification in general requires that devices are able to deliver gain when loaded by relatively high load impedances. Voltage gain with a high, or infinite, output load, is therefore a figure of merit that directly reflects the usefulness of a device in amplifiers and most other fundamental analog/RF building blocks such as oscillators, sample-and-holds, and frequency converters.

dx.doi.org/10.1021/nl2016637 |*Nano Lett.* 2011, 11, 3690–3693

Measuring a device with a high impedance requires a measurement technique which eliminates the 50 ohm load of a network analyzer. At low frequency, an oscilloscope with a high impedance input can be used to measure the amplifier output, but it has limited dynamic range and bandwidth, so a different technique is required. The graphene FET was measured as a common-source amplifier (Figure 4a), biased in saturation near the maximum g_m. The transistor was probed with conventional microwave probes, and biases were applied through bias tees. The gate was driven by a sine wave of adjustable frequency. To present a high impedance load to the device, a short length of unterminated coaxial cable was attached to the output. This presents a high impedance at frequencies corresponding to multiples of the wavelength divided by two. The input and output voltages were measured directly using the signal generated with a high impedance active microprobe having 25 GHz bandwidth placed at the gate and drain terminals of the device. The microprobe output signal was measured with a spectrum analyzer, and voltage gain was determined from the difference of measured input and output signals

Figure 4b shows the relative gain versus input power at a single frequency, showing linear amplification over a 4 orders of magnitude range until the compression point is reached. With the signal level at −17 dBm (30 mV-rms), below the compression point the voltage gain is shown as a function of frequency up to 6.5 GHz in Figure 4c. This graphene amplifier exhibits ∼5 dB low frequency gain with 3 dB bandwidth greater than 6 GHz. The solid line indicates the gain of the amplifier that was obtained by simulation using the measured s-parameters. In the simulation, the small-signal characteristics of the device are represented by measured 2-port s-parameters, and the load consists of the probe parasitic capacitance and the measured impedance presented by the open-ended transmission line. As shown in Figure 4c, the simulations are in good agreement with the measurements, validating the experimental demonstration of this graphene-based amplifier. The simulation also shows the device is capable of voltage amplification for frequencies exceeding 15 GHz. Compared with previously reported graphene analog circuits that always show the attenuation of the signal, this is the first time an AC gain has been reported.

In summary, a high-frequency amplification circuit using graphene devices has been demonstrated. The amplifier is the first graphene circuit to show AC voltage gain, an attribute required in most analog circuits. An embedded gate structure with an aggressively scaled gate oxide leads to clear current saturation, enabling high-frequency voltage gain. In addition, fabrication of this graphene amplifier in a wafer-scale platform sets an important milestone for transitioning this 2D material into a viable technology.

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ACKNOWLEDGMENT

Authors acknowledge support by Defense Advanced Research Projects Agency under contract FA8650-08-C-7838 through the Carbon Electronics for RF Applications program. The views expressed are those of the author and do not reflect the official policy or position of DARPA.

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