Graphene Technology with Inverted-T Gate and RF Passives on 200 mm Platform

Shu-Jen Han, Alberto Valdes-Garcia, Ageeth A. Bol, Aaron D. Franklin, Damon Farmer, Ernst Kratschmer, Keith A. Jenkins, Wilfried Haensch

IBM T.J. Watson Research Center, Yorktown Heights, NY 10598

TEL:+1-914-945-2876 EMAIL:sjhan@us.ibm.com

ABSTRACT

Wafer-scale graphene devices processed entirely in a standard *200 mm* silicon fab are demonstrated for the first time. New embedded gate structures enable full saturation of the drain current in graphene FETs with sub-µm channels, resulting in high intrinsic *voltage gain*. In addition, passive devices were monolithically integrated with graphene transistors to form the first GHz-range graphene IC using large-scale CVD graphene. The demonstration of high performance graphene FETs and IC fabricated using a 200 mm platform is a major step in transitioning this promising material from a scientific curiosity into a real technology.

INTRODUCTION

Graphene, a single sheet of carbon atoms bonded in a hexagonal lattice, exhibits some remarkable electrical properties, including impressively high current density, mobility and saturation velocity [1-3]. Several recent graphene RF reports have moved beyond device-level demonstration (i.e. f_T, f_{max}) and showed functional graphene circuits, especially for analog/RF applications [4-6]. Despite this progress and the extensive studies of graphene FETs, most experiments to date have been conducted using small-scale graphene films realized with *off-line* process flows. In particular, the introduction of large-scale graphene into a standard silicon fab has not yet been established. In this paper, we demonstrate for the first time fabrication of graphene devices in a full 8" wafer scale context. A novel inverted-T gate enabled by the wafer-scale process significantly reduces the device gate resistance. This embedded gate structure also allows an ultrathin dielectric to be employed in our devices, which contributes to both drain current saturation and high voltage gain. In addition, the first integrated graphene frequency multiplier is presented. The multiplier IC shows GHz operation frequency and superior temperature stability over conventional Si-based technologies.

GRAPHENE DEVICE

Establishing a high-quality ALD or CVD gate dielectric on graphene's inert surface remains one of the most challenging issues in graphene device fabrication. CVD-grown graphene, however, has the unique ability to be transferred onto almost any substrate, including wafers with pre-defined embedded gate structures—completely eliminating the need of depositing a dielectric on graphene. Our developed process flow for graphene FETs and RF passives is shown in **Fig. 1**. First, deep trench was formed in 1 µm thick SiO_2 on a high resistive Si substrate by reactive ion etching (RIE). After ~400 nm thick W deposition, the wafer was chemical-mechanical polished. CVD HfO_2 was deposited as the gate dielectric. Contact area to the pad of the embedded gate was etched open. Large area CVD

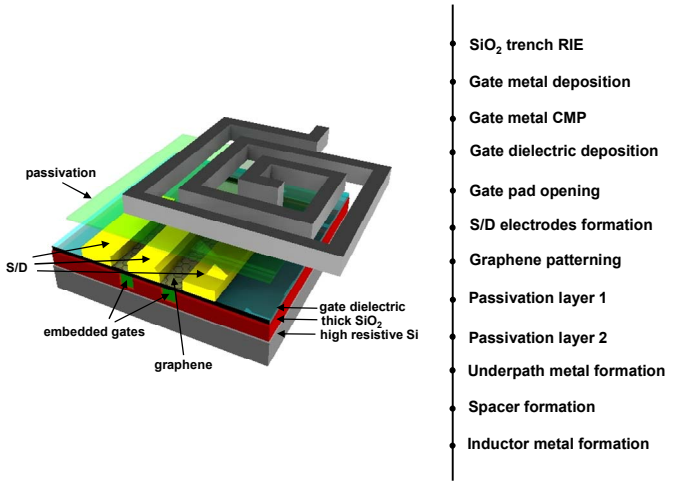


Fig. 1 Schematic of graphene IC and the integration flow. The fabricated devices were protected by two layers of passivation. Finally, to form an RF IC, an inductor was integrated with a FET device.

graphene was then transferred onto the 8" wafer. Pd contact stacks were formed and graphene was patterned. The embedded gate enables an ultrathin gate dielectric (<40 Å HfO_2), with the potential for further scaling. To reduce the gate resistivity (to improve device RF performance), a novel inverted-T gate structure was also developed to maximize the cross-sectional area of the gate. The cross-sectional SEM image of such a gate is shown in **Fig. 2**. Compared to our first-generation embedded gate structure [7], this inverted-T gate reduces the gate resistivity by ~65% for the 300nm channel device (the shortest channel length in the current mask design), and we expect even more improvement for devices with shorter channels. Compared to the top-gate structure, our embedded gate design largely simplifies the process of making T-shaped gates and avoids the parasitic capacitance between gate and S/D electrodes.

With the embedded gates completed, single-layer, large area CVD-grown graphene film was transferred to cover the 200 mm substrate. The transferred graphene film has good uniformity across the wafer, as can be seen in the Raman data shown in **Fig. 3**. The 2D/G ratio suggests CVD graphene film is predominantly a monolayer. Good film quality is also confirmed by a reasonably low D peak across the wafer. **Fig. 4** shows a photograph of a fully processed wafer and SEM images of a 2-finger device.

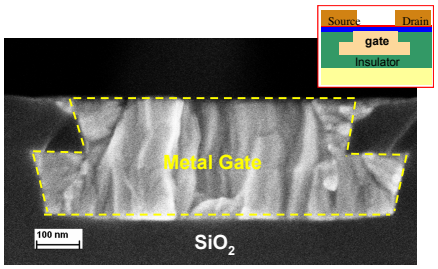


Fig. 2 Cross-sectional SEM image of post-CMP wafer showing the inverted-T gate structure.

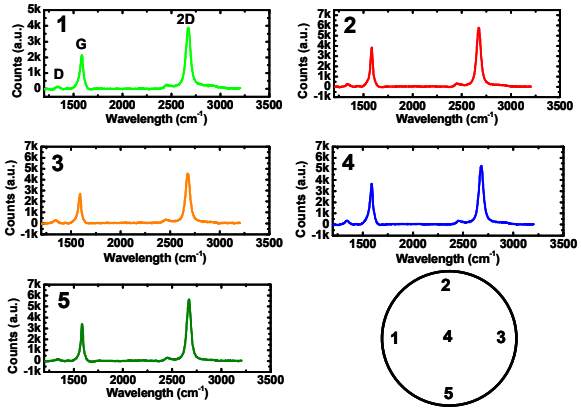


Fig. 3 Raman spectra mapping of large area CVD graphene film on 200 mm wafer. Good uniformity is observed across the wafer.

It was found that a solid passivation is especially important in our embedded gate devices for two reasons: (1) it reduces the hysteresis and improves the device stability, and (2) it protects graphene from damage during the fabrication of passive devices. Our passivation consists of a polymer#1 (to preserve graphene mobility), dielectric#1, and dielectric#2 (to cover sidewalls of polymer#1 and dielectric#1). **Fig. 5 (a)** shows transfer curves from a graphene FET, and it is evident that the passivation substantially reduces the hysteresis. The device hysteresis can be partially attributed to the surface-molecule assisted charge transfer between graphene and charge traps at dielectric interface. The effectiveness of hysteresis reduction can be clearly seen from the distribution plot in **Fig. 5 (b)** where the average hysteresis is reduced by nearly 80% after passivation.

Fig. 6 (b) displays the distribution of the extrinsic transconductance (g_m) from devices with the same channel length (500nm) and three different widths (5µm x 2, 15µm x 2, and 25µm x 2) on the same wafer. It shows three distinct peaks corresponding to three different device sizes, where small devices exhibit better performance than larger devices (raw transfer curves of all three device geometries are also shown in **Fig. 6 (a)**). We attribute this difference to the lower chance of defects (e.g. domain boundary or wrinkles) occurring in the channel region in smaller devices. Nevertheless, all of the measured devices across the 8" wafer were functional, which demonstrates the robustness of the process presented here.

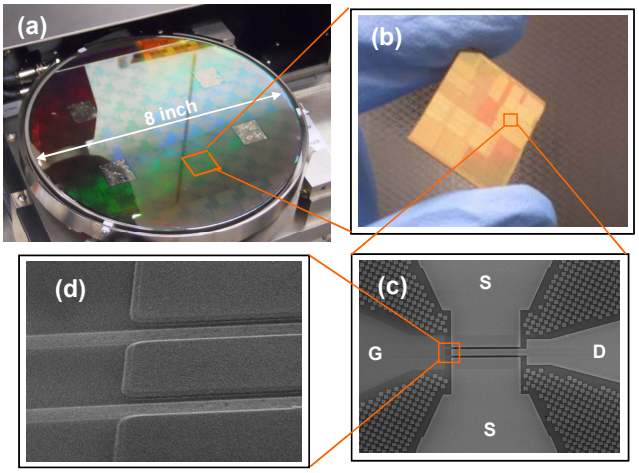


Fig. 4 Photographs of (a) an 8" graphene FET wafer and (b) single die (c) SEM image of a typical fully-processed device. (d) Enlarged view of the device showing the embedded gate structure with 2-finger design. The process was completely fabricated in 200 mm fab except the CVD graphene transfer.

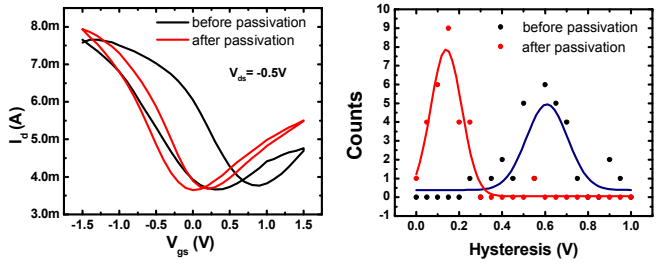


Fig. 5 (a) Transfer curves of a typical device before and after the completion of the passivation layers. Hysteresis is largely reduced with the proper passivation. (b) Reduction of hysteresis by device passivation in a large set of devices.

Typical DC characteristics of a 5µm x 2 wide device are shown in **Fig. 7**. I_d-V_{gs} curves in **Fig. 7 (a)** show that the shift of minimum conduction point (dashed line) is consistently equal to ½ of the applied V_{ds} due to graphene's ambipolar property [8]. Usually, this shift has little effect when a thick gate dielectric is employed; however, with an aggressively scaled dielectric (as in our embedded gate structure), the required gate bias becomes comparable to the drain bias, and the curves move closer to each other with increasing drain bias. This curve shifting translates into a clear drain current saturation, which can be seen in **Fig. 7 (b)**, even though graphene has no bandgap. The resulting low output conductance (g_{ds}) is essential in most analog/RF circuit designs since the intrinsic voltage gain (G_{in}) (clearly present in our devices as shown in **Fig. 7 (c), (d)**) is determined by g_m/g_{ds}.

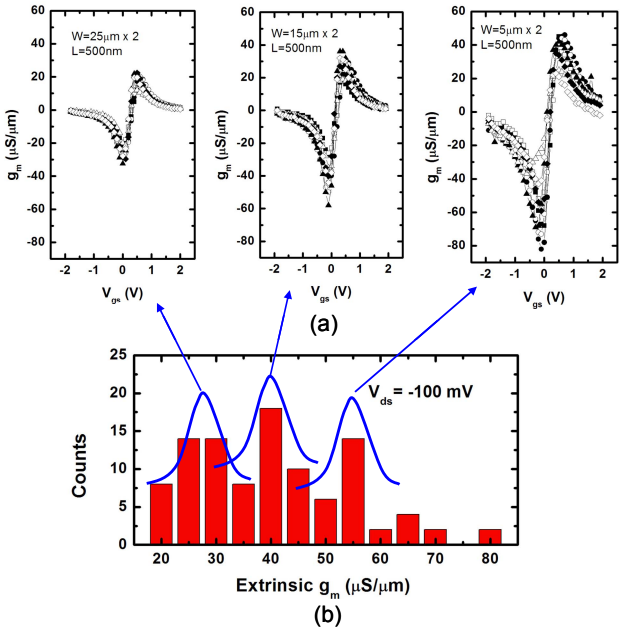
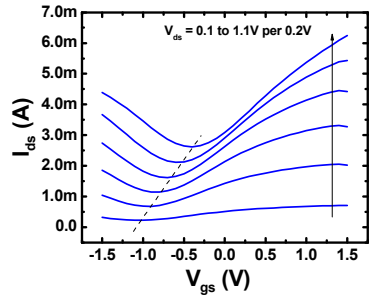
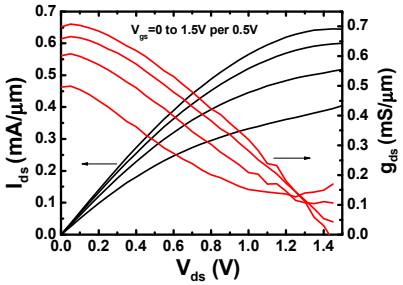


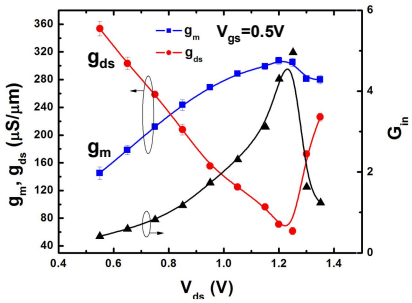
Fig. 6 (a) Raw transfer curves of devices with 25µm x 2 (left), 15 µm x 2 (middle), and 5µm x 2 (right). (b) Distribution of normalized extrinsic transconductance for over 100 devices. Three distinct peaks correspond to three different device sizes in the measurement. Size dependence of the device performance can be clearly seen where smaller devices show higher g_m than larger devices. This behavior can be attributed to the lower chance of defects (e.g. domain boundary) occurring in the channel region in smaller devices.



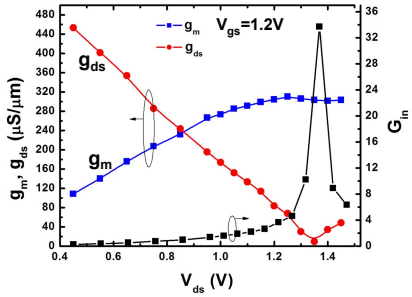
(a)



(b)



(c)

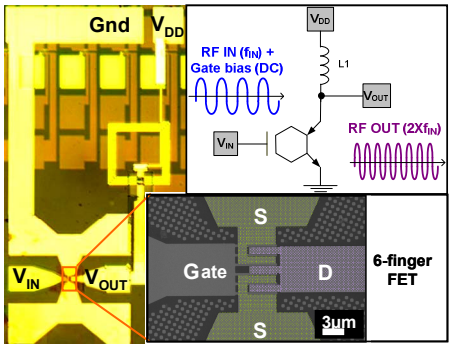


(d)

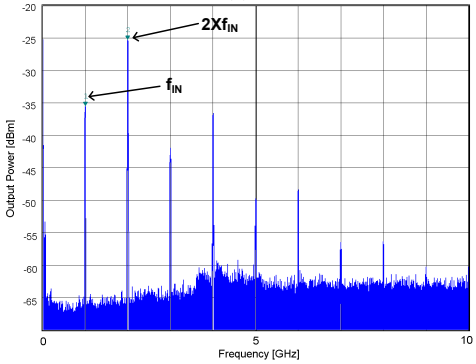
Fig. 7 (a) I_d-V_{gs} at different V_{ds} for a 5μm x 2 wide device with 500nm channel length. (b) Output characteristics of the same device. Strong current saturation and desired low g_{ds} are achieved. (c) g_m, g_{ds}, and intrinsic voltage gain (G_{in}=g_m/g_{ds}) as a function of V_{ds} at V_{gs}=0.5V. (d) g_m, g_{ds}, and G_{in} at V_{gs}=1.2V.

Fig. 7 (c) and (d) shows g_m, g_{ds}, and G_{in} as a function of V_{ds} at V_{gs}=0.5 V and 1.2 V respectively. Higher V_{gs} yields better saturation and a higher peak gain, which is about 34 for 1.2 V V_{gs}. From these curves, it is evident that these embedded gate graphene FETs can easily achieve G_{in} > 1 at a wide range of bias conditions.

GRAPHENE IC



(a)



(b)

Fig. 8 (a) Photograph of graphene IC using CVD graphene and embedded gates. Inductors were monolithically integrated with graphene FETs and the circuit was measured as a frequency doubler. A six-finger device was used in the circuit. (b) Captured image from the spectrum analyzer during the circuit operation. With input power of 0 dBm at 1GHz, the conversion gain is ~ -25 dB

To demonstrate the usefulness of this technology in RF circuit applications, a 4-turn inductor (targeting L=5nH) was monolithically integrated with a 6-finger graphene FET (**Fig. 8 (a)**). The main inductor loop was made with > 1μm thick Al. The fabricated IC was measured as a frequency doubler. The measured output power spectrum for an input frequency (f_{IN}) of 1 GHz is shown in **Fig. 8 (b)**. This doubler features a conversion gain of ~-25 dB for an output frequency of 2 GHz with a rejection of the fundamental tone and other frequency components of more than 10 dB—significantly better than previous reports [4]. The integrated inductor provides a band-pass response to the doubler output and additional rejection of unwanted tones. Within the range of 2 to 5 GHz the 2nd harmonic output power shows a variation of < 1 dB. Since the IC operation relies on the ambipolar property of graphene FETs, the operation modes can be tuned by selecting the gate bias point as shown in **Fig. 9**. As expected, the circuit shows the highest conversion gain and spectral purity when the gate bias is close to the Dirac point (point 2). The circuit starts to lose its frequency doubling property when it is biased away from the Dirac point (point 1, 3).

Fig. 10 shows the measured performance over temperature. Both the power at the second harmonic and the ratio between the second harmonic and the fundamental show less than +/- 1 dB variation from room temperature to 200 °C. The nearly-constant frequency doubler performance over such a wide temperature range indicates that the graphene transconductance in both p and n branches is temperature independent in this

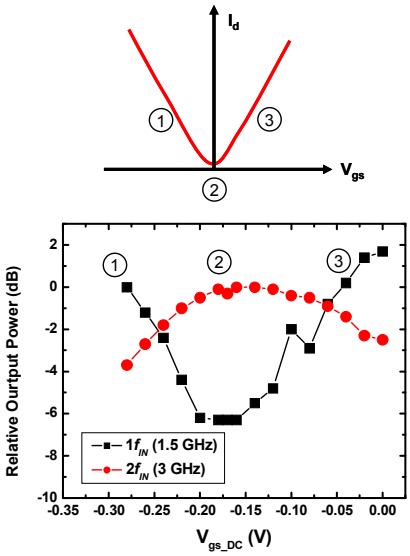


Fig. 9 Measured relative output power at f_{IN} (1.5GHz) and $2f_{IN}$ (3GHz) as a function of DC gate bias for the graphene-based integrated frequency doubler.

range. To our knowledge, this is the first demonstration of this property in CVD graphene.

CONCLUSION

We have shown 200 mm wafer-scale graphene RF devices and integrated circuits using a completely CMOS-compatible process flow. These sub-µm graphene FETs made from large-scale CVD graphene show clear drain current saturation and exhibit high intrinsic voltage gain. This work is a major step in advancing the maturity of large-scale graphene technology.

ACKNOWLEDGEMENTS

The authors acknowledge support by Defense Advanced Research Projects Agency under contract FA8650-08-C-7838 through the Carbon Electronics for RF Applications program. The views expressed are those of the author and do not reflect the official policy or position of DARPA. We would also like to acknowledge Dr. C.Y. Sung, Dr. Y. Sun, Dr. X. Li and staff in IBM T.J. Watson Microelectronics Research Laboratory (MRL) for their technical support.

REFERENCES

[1] K. C. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, no. 5696, pp. 666–669,Oct. 2004.

[2] B. Huard, J. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon, "Transport measurements across a tunable potential barrier in graphene," *Phys. Rev. Lett.,* vol. 98, no. 23, p. 236 803, Jun. 2007.

[3] M. C. Lemme, T. Echtermeyer, M. Baus, and H. Kurz, "A graphene field effect device," *IEEE Electron Device Lett*., vol. 28, no. 4, pp. 282–284, Apr. 2007.

[4] H. Wang, A. Hsu, K. K. Kim, J. Kong, T. Palacios, in Electron Devices Meeting, 2010 (IEDM 2010), IEEE International, San Francisco, December 2010, pp. 23.6.1 - 23.6.4.

[5] S.-J. Han, K. A. Jenkins, A.Valdes-Garcia, A. D. Franklin, A. A. Bol, and W. Haensch, "High-Frequency Graphene Voltage Amplifier," *Nano. Lett*., vol. 11, no. 9, pp. 3690-3693, Aug. 2011

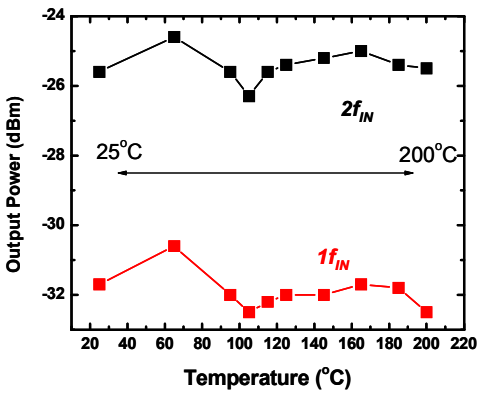


Fig. 10 Measured frequency doubler performance over temperature for f_{IN}=1GHz. This is an important advantage of this technology for high-temperature applications.

[6] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, P. Avouris, K. A. Jenkins, "Wafer-scale Graphene Integrated Circuit.," *Science*, vol. 332, no. 6035, pp. 1294-1297, Jun. 2011.

[7] S.-J. Han, J. Chang, A.D. Franklin, A.A. Bol, R. Loesing, D. Guo, G.S. Tulevski, W. Haensch, Z. Chen, "Wafer scale fabrication of carbon nanotube FETs with embedded poly-gates," *IEDM Tech. Dig*. 2010, pp. 9.1.1-9.1.4, Dec. 2010.

[8] S.-J. Han, Z. Chen, A.A. Bol, Y. Sun, "Channel-Length-Dependent Transport Behaviors of Graphene Field-Effect Transistors," *IEEE Electron Device Lett.*, vol. 32, pp. 812-814, Apr. 2011.