Wafer Scale Fabrication of Carbon Nanotube FETs with Embedded Poly-gates

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ABSTRACT

One critical factor that determines the feasibility of employing carbon nanotubes as channel materials for post-silicon logic devices is the process compatibility to the current CMOS process flow. We show a wafer-scale integration scheme of carbon nanotube field-effect transistor (CNFET) that is performed by 8" production tools. High density CNT arrays were transferred on the processed wafer, and high performance CNFET with an excellent subthreshold slope (88 mV /decade) is demonstrated. We further show that the work-function tuning enabled by the conventional gate doping can be achieved in our novel embedded poly-Si gate structure. Approximate V_t change of 0.6V, from n-gate to p-gate, is observed. The V_t shift being smaller than the gate work function difference can be attributed to the Fermi level pinning between poly-Si and high-k interface.

INTRODUCTION

Carbon nanotube has been identified as one of the promising candidates for future nano-electronic applications. Despite exceptional transport properties in carbon nanotubes [1, 2], large-scale integration of CNFETs has not yet demonstrated, which hinders further development of the technology. Up to date, all nanotube devices and circuits were fabricated in off-line tools at small scales due to process compatibility issues with the state-of-art CMOS technology. In this paper, we report for the first time a wafer-scale fabrication of high performance CNFETs using an 8" production line. For electronic devices using carbon (CNT or graphene) as conduction channels, the lack of high quality gate dielectric is always a bottleneck for further device optimization. Typically, the use of thick dielectric or a nucleation layer before dielectric is required to ensure uniform coverage of dielectric on the carbon surface [3]. A novel embedded poly-Si gate structure is employed to provide excellent electrostatics in the devices and the compatibilities with CMOS processes. In addition, the first-ever measured CNFET threshold tuning through poly-Si gate doping is presented. Lastly, the role of hysteresis in CNFET device measurements is also described in details.

DEVICE FABRICATION

Fig. 1 shows the key process steps of our device fabrication. Si wafer with 1 μm thermal oxide served as the starting substrate. A photolithography step followed by reactive ion etch (RIE) removed 250 nm SiO2 to define trenches for the poly-Si gates. Before the poly-Si deposition, a thin nitride liner (~200 Å, RTCVD) was inserted to prevent the loss of gate dopants into the

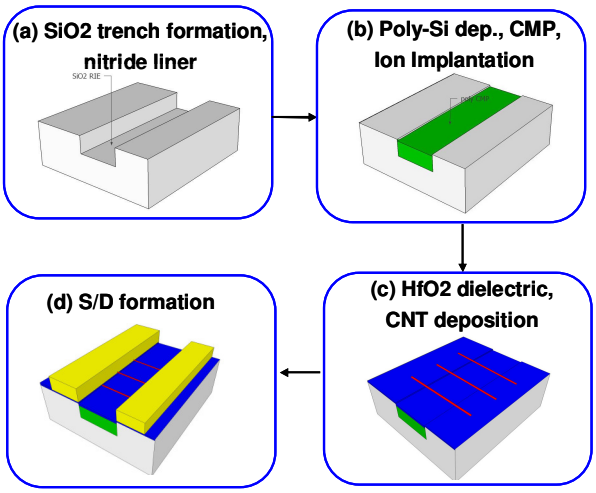

Fig. 1 Schematic of the simplified process flow: (a) Deep trench was formed in 1 μm thick SiO_2 by RIE. 200 Å nitride liner then was deposited. (b) After ~500 nm thick poly-Si deposition, the wafer was CMPed. As and BF_2 were implanted for n- and p- gate, followed by RTA. (c) 44 Å CVD HfO_2 was deposited as gate dielectric. CNTs were placed perpendicularly to the embedded gate structure. (d) Pd contact stacks were formed to obtain low Schottky barrier for PFET.

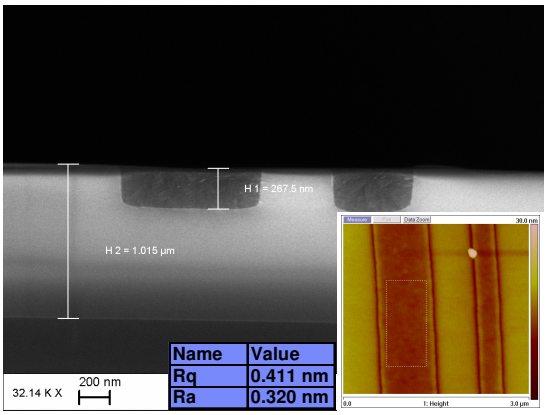

Fig. 2 Cross-sectional SEM image of post-CMP wafer. The embedded gate is ~250 nm thick poly-Si with the average surface roughness < 5 Å after CMP (inset, measured by AFM).

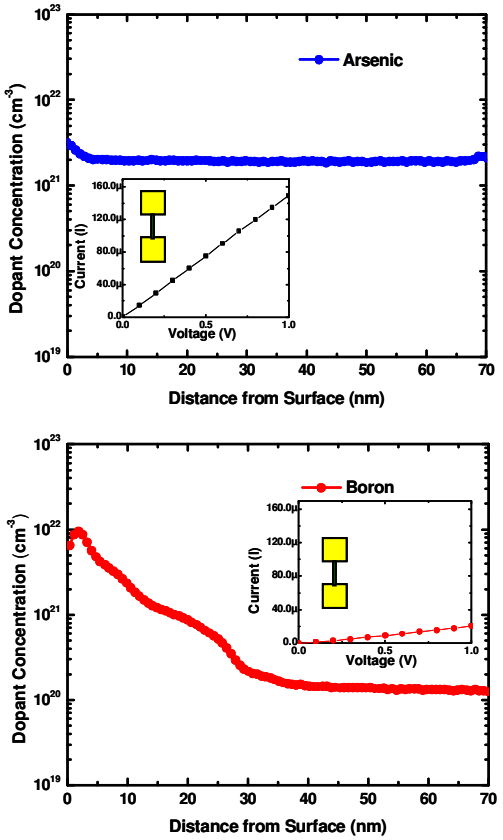

Fig. 3 SIMS profiles of (top) As and (bottom) B after RTA. 2 steps implantation were employed (low energy + high energy) to reduce both poly-depletion effect and gate sheet resistance. The surface dopant concentration was well above 10^{21} cm^{-3}. Resistivity can be calculated from I-V of the wire structure on the same wafer (inset).

surrounding SiO_2. 500 nm LPCVD poly-Si was then deposited, and the wafer was sent for chemical-mechanical polishing (CMP).

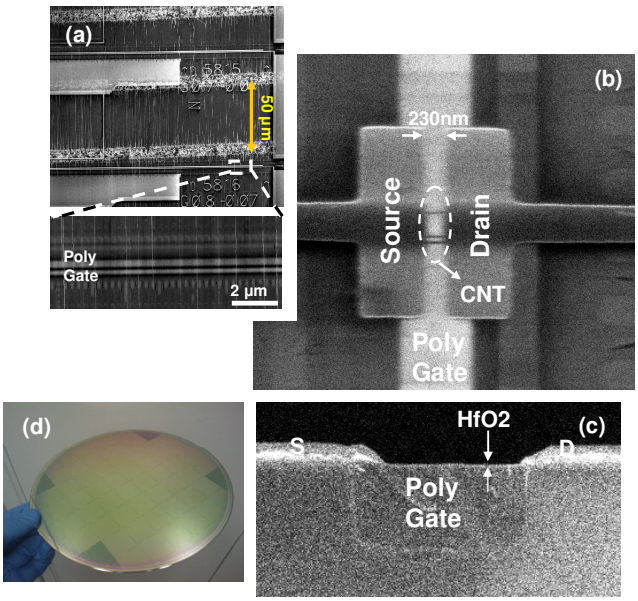

Fig. 4 (a) SEM image of transferred aligned CNTs on the wafer with embedded poly gates. (b) Top view and (c) cross-sectional view of a typical fully-processed device. (d) Fully-processed 8" wafer with CNFETs. The process was completely done using 8" production line tools except the CNT transfer.

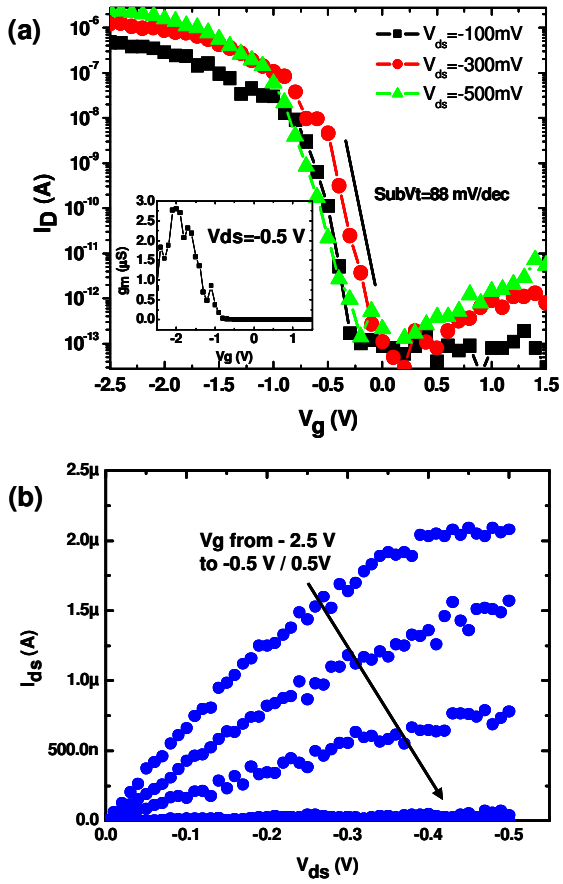

Fig. 5 Characteristics of single tube PFET with a channel length of 230 nm. (a) Subthreshold characteristic with different drain bias conditions, which shows an excellent inverse subthreshold slope (~88 mV /decade). With 44 Å HfO_2, the gate leakage was well below 10^{-12} A. (Inset) transcontance vs. gate bias. (b) I_{ds} – V_{ds} curves under various V_g. The saturation current is ~2 μA.

Fig. 2 shows a cross-section SEM image of poly gates after CMP. Smooth poly surface (average roughness < 5 Å from atomic force microscope) was achieved in CMP to ensure a high quality dielectric deposition. Because our gate process reversed the conventional top-gate scheme, an ultra low energy ion-implantation with high doses was used to form heavily degenerated n- and p-type doping near the surface. To reduce the gate resistivity, a second implantation with higher energy was performed. Fig. 3 shows doping profiles of both n-gate and p-gate from secondary ion mass spectrometry (SIMS) after rapid thermal annealing (RTA). A flat profile in As-doped gate is observed due to the higher annealing temperature (1050 °C vs. 950 °C for BF2 gate). The resistivities of n- and p-gate are measured to be 2 and 16 mΩ-cm, respectively. Since there are no thermal budget and dopant penetration concerns in our process flow, the gate resistance can be further improved by the optimization of RTA/implant conditions. Pure metal gates (with proper gate workfunctions) can also be used to provide better gate resistance, however, the material compatibility issue to current CMOS process equipments needs be solved.

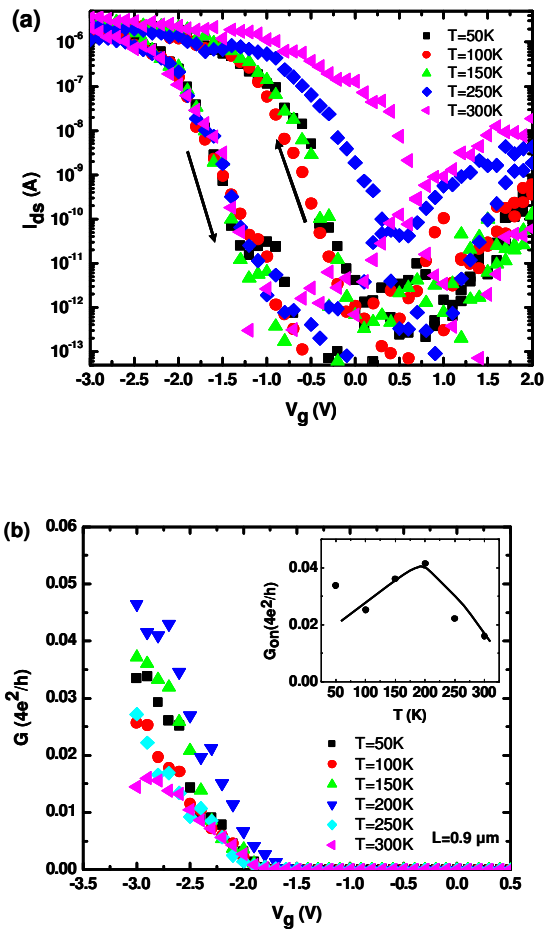

Fig. 6 (a) Measured I_{ds} - V_g at various temperatures. The device shows positively shifted gate hysteresis which has been attributed to the charge transfer between CNT and charge traps at dielectric/ambient interface. (b) Conductance as a function of gate voltage for a long channel device (L=0.9 μm) measured at various temperatures.

After native oxide removal, 44 Å CVD HfO_2 was then deposited at 500 °C. The method we used to prepare carbon nanotube array on substrates is similar to ref [4]. Aligned CNT arrays grown on single-crystal quartz were transferred to our wafer, forming single- or multi-CNT channels per device for high current output, as shown in Fig. 4(a) and (b). Finally, contact metals of 5Å Ti/300Å Pd/200Å Au were formed to complete the CNFETs. Note here, the characteristics presented later are intentionally obtained from devices with single CNTs, in order to minimize the complexity of quantifying the gate doping induced threshold voltage (V_t) control.

EXPERIMENTAL RESULTS

Fig. 5 (a) shows the subthreshold characteristic of an embedded poly-Si gated single CNT device with channel length of 230nm. All the measurement is done at room temperature in N_2. In Schottky barrier devices such as CNFETs, the inverse subthreshold slope (SS) is proportional to the square root of the gate dielectric thickness (T_{ox}) [5]. It is very different to the conventional well-behaved fully depleted MOSFET in which the inverse SS is independent of the gate dielectric thickness. Thanks to the aggressive dielectric scaling in our embedded gate structure, the device possesses an excellent subthreshold swing of 88 mV/dec with an I_{on}/I_{off} ratio above 10^6. A peak trans-conductance of 2.9 μS (at Vds= -0.5 V) also shows the high performance of the device. Fig. 5 (b) shows the output characteristics for the same device.

Before we can investigate the V_t control through gate workfunction, a reliable V_t reading has to be established. It is well known that one-dimensional nano-electronic devices suffer from hysteresis more severely than conventional planar devices due to the enhanced gate field around the channel body. Measured I_{ds} - V_g from a long channel device at various temperatures under vacuum are plotted in Fig. 6 (a). It is clearly seen that curves swept from negative V_g are insensitive to temperature changes. On the contrary, strong temperature dependence of curves swept from positive V_g is observed. It suggests a strong electron trapping at the dielectric interface, which had usually been attributed to water molecules [6]. We also notice a much more suppressed hysteresis at low temperatures which could be due to the water freeze. On state conductance shows metallic behavior above 200K which shows near-ohmic contacts in our devices. The conductance decrease at

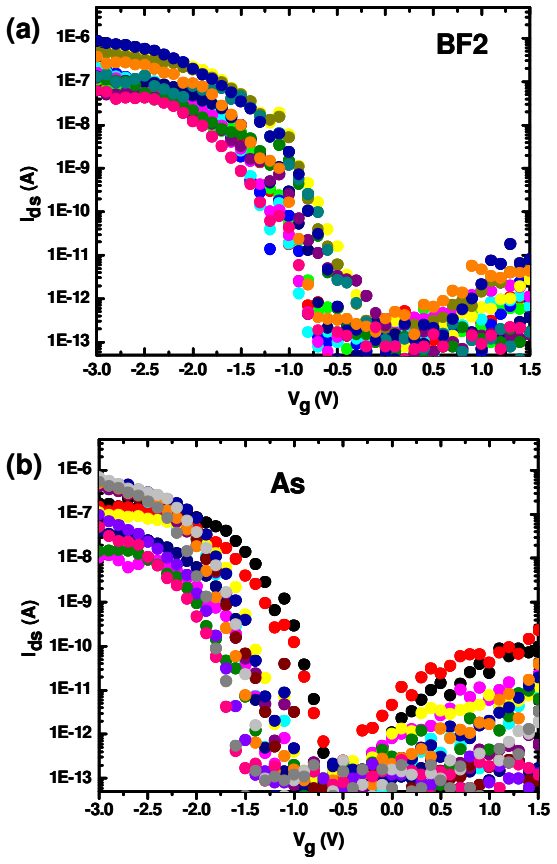

Fig. 7 Measured I_{ds} - V_g from devices with (a) BF2 doped embedded poly gates, and (b) As doped gates. Both show excellent I_{on}/I_{off} ratio (> 10^5). The testing was carried out from negative V_g to positive V_g to eliminate the hysteresis effect (Fig. 6). The rather large spread of curves reflects the variation of CNT diameters.

lower temperature could be attributed to weak localization due to defects.

Fig. 7 (a) and (b) demonstrate fully functional CNFETs with p-poly gate and n-poly gate, respectively. All measurements were performed from negative V_g to positive V_g to minimize the hysteresis effect. The rather large spread of measured curves is attributed to the diameter (inversely proportional to band gap) distribution in CNTs. Two datasets are plotted together in Fig. 8 (inset) and it shows clear V_t shift due to the gate workfunction difference. BF2 implantation lowers PFET V_t. To quantify the V_t shift, characteristics of two devices with the same diameter (same bandgap) and opposite gate types are plotted in Fig. 8. Approximate V_t change of 0.6V is observed. The V_t shift being smaller than the gate work function difference can be attributed to the Fermi level pinning between poly-Si and high-k interface.

CONCLUSION

We have shown the first-ever attempt of fabricating CNFETs with wafer scale using a completely CMOS compatible process flow and novel embedded poly-Si gate structures. An aggressively scaled gate dielectric with high quality can be formed with this gate structure and high performance CNFET is demonstrated. This work brings us one step closer to the realization of very large scale complementary CNT integrated circuitry.

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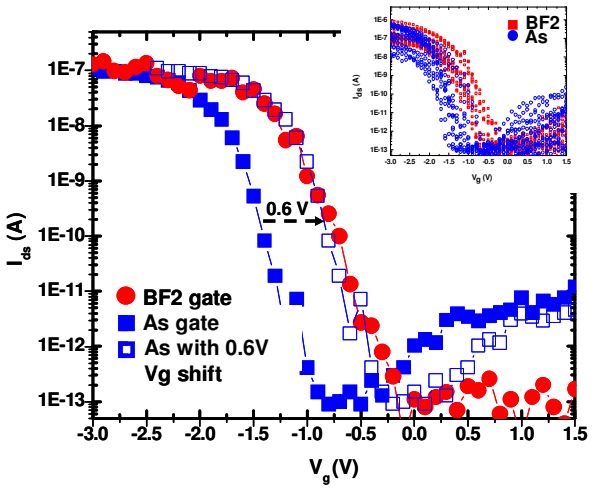

Fig. 8 I_{ds} - V_g from devices with n- and p- gate. Positive V_t shift (~0.6 V) was clearly observed from devices with BF2 doped gates. Fermi-level pinning between poly-Si and HfO2 might result in the smaller V_t shift.