

Toward surround gates on vertical single-walled carbon nanotube devices

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The one-dimensional, cylindrical nature of single-walled carbon nanotubes (SWCNTs) suggests that the ideal gating geometry for nanotube field-effect transistors (FETs) is a surround gate (SG). Using vertical SWCNTs templated in porous anodic alumina, SGs are formed using top-down processes for the dielectric/metal depositions and definition of the channel length. Surround gates allow aggressive scaling of the channel to 25% of the length attainable with a bottom-gate geometry without incurring short-channel effects. The process demonstrated here for forming SGs on vertical SWCNTs is amenable for large-scale fabrication of multinanotube FETs. © 2009 American Vacuum Society. [DOI: 10.1116/1.3054266]

I. INTRODUCTION

Nanostructures such as nanowires and nanotubes enable fundamental performance advantages over bulk Si for next generation field-effect transistors (FETs)—including decreased gate delay,¹ enhanced mobility,² lower power operation,^{3,4} and greater opportunity to scale channel length.⁵ Many of these advantages draw from the low-dimensional electrostatics and quantization of electron states that are caused by the decreasing dimensionality of a material to form a nanostructure. Single-walled carbon nanotubes (SWCNTs), which structurally are rolled graphene sheets with no edge states and diameters ranging from 1 to 3 nm, exhibit excellent one-dimensional (1D) electrostatics that allow for the most aggressive channel length scaling among nanomaterials considered for nanoelectronic applications.⁵

To take full advantage of the superior scaling capability of SWCNTs, a surround (i.e., coaxial, annular, wrap-around) gate should be employed to obtain optimal control over the energy bands in the nanotube channel. Other studies have demonstrated the implementation and advantages of surround gates (SGs) for nanowire FETs by using the rigid structure of vertical nanowires to template the dielectric and gate metal deposition.^{6–8} However, applying SGs to SWCNTs has been proven difficult because of their lack of rigidity and small diameters. Forming SGs to planar,

substrate-supported nanotubes is infeasible because their interaction with the substrate forces the formation of omega-shaped gates that cover only the sides and top of the nanotube. One report to date involving SGs on SWCNTs required the suspension of the nanotubes over long trenches where the SG was formed, followed by random dispersion of the nanotube composites to assemble the FETs in a separate step.⁹ Unfortunately, the fabrication process did not allow for accurate scaling of the channel length for these externally assembled devices. Vertical SWCNTs (v-SWCNTs) that are freestanding and supported in a template would provide access to the entire nanotube for applying a completely surrounding dielectric and metal gate as well as improved control over device placement and channel length.

Recently, templated synthesis,¹⁰ backcontact formation,^{11,12} and length control of v-SWCNTs supported in porous anodic alumina (PAA) have been reported.¹³ Using these templates of v-SWCNTs, we present the fabrication of surrounding dielectrics and gates on nanotubes along with a facile means for controlling the device channel length. An inert gas ion bombardment etch is used to define the final channel length to within a very narrow range (± 15 nm) over an entire chip and in a single step, thus eliminating the need for complex and expensive lithography. The combination of surround gates on v-SWCNTs and a method for scaling the channel length at the wafer level provides a platform for realizing SWCNT-FETs that take full advantage of the 1D electrostatics.

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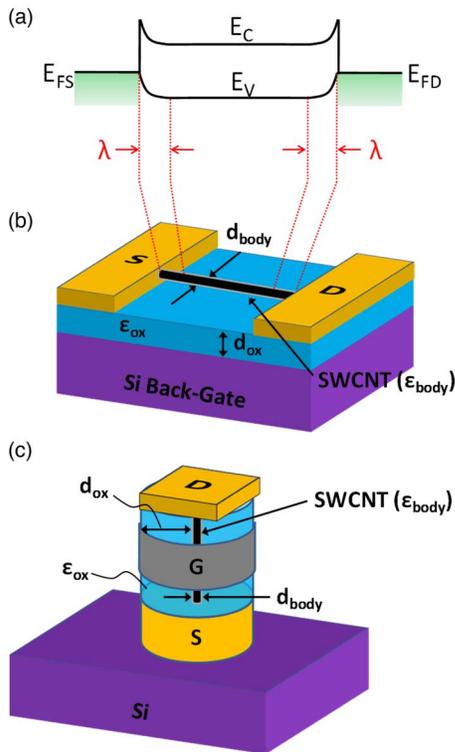


FIG. 1. (Color online) (a) Schematic band diagram of a hypothetical SWCNT-FET illustrating the screening length (λ) in the channel. SWCNT-FET schematics with (b) a BG configuration and (c) a SG configuration.

II. ADVANTAGES OF SURROUND GATES

The screening length (λ) is an intrinsic property of a device configuration that represents the natural length over which potential is dropped between two electrically different materials (e.g., p - n or metal-semiconductor junctions). A similar intrinsic length often introduced in bulk semiconductor electrostatics is the Debye length, which traditionally represents some factor of the depletion width of a p - n junction in thermal equilibrium for a semiconductor with a particular doping level.¹⁴ The Debye length is a device parameter that depends on doping and temperature, while the screening length λ is an intrinsic parameter that depends only on dielectric/channel properties and thicknesses.⁵ For nanoscale devices, the smaller of these two lengths will determine the distance over which the bands bend—for thin body devices (e.g., nanowires or nanotubes) the doping would have to be very high to render a Debye length shorter than λ .

In nanoelectronic devices, λ offers a metric for determining how aggressively a device's channel length can be scaled down without incurring deleterious short-channel effects, such as high leakage currents and drain-induced barrier lowering.^{2,5} One proposed rule of thumb for scaling nanoelectronics is to keep the channel length greater than 3λ in order to maintain long-channel device behavior.⁵ Figures 1(a) and 1(b) illustrate the screening length for a hypothetical SWCNT-FET. For any 1D cylindrical channel (nanotube or nanowire) in a bottom-gate (BG) configuration, λ can be found using:¹⁵

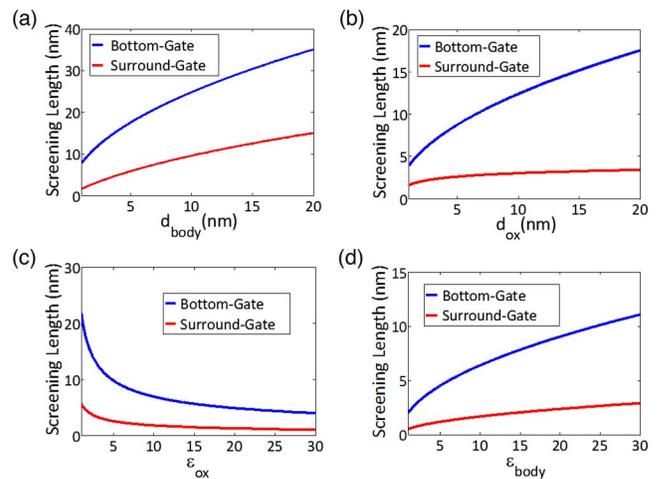


FIG. 2. (Color online) Plots of the screening length vs (a) channel body thickness (i.e., nanowire or nanotube diameter), (b) gate oxide thickness, (c) gate oxide dielectric constant, and (d) body dielectric constant. Except as noted, the following constants were used for the relative simulations: $\epsilon_{ox} = 3.9$, $\epsilon_{body} = 30$, $d_{ox} = 8$ nm, and $d_{body} = 2$ nm.

$$\lambda_{BG} = \sqrt{\frac{\epsilon_{body} d_{ox} d_{body}}{\epsilon_{ox}}} \quad (1)$$

In Eq. (1), ϵ_{ox} is the dielectric constant of the gate dielectric, ϵ_{body} is the dielectric constant of the channel material (nanotube or nanowire), d_{ox} is the gate dielectric thickness, and d_{body} is the thickness (diameter) of the nanomaterial.

A schematic for a SG SWCNT-FET is shown in Fig. 1(c). As compared to the BG geometry, the SG improves control over the electrostatics,¹⁵ and the potential distribution in the channel changes to give the following relation for the screening length:

$$\lambda_{SG} = \sqrt{\frac{\epsilon_{body} d_{body}^2}{8\epsilon_{ox}} \ln\left(1 + \frac{2d_{ox}}{d_{body}}\right)} \quad (2)$$

Figure 2 shows the variation of screening length from the two device geometries as a function of the parameters d_{body} , d_{ox} , ϵ_{ox} , and ϵ_{body} . These plots clearly illustrate the advantage of a SG geometry, which allows for a channel length nearly an order of magnitude less than a BG geometry while still avoiding short-channel effects (based on the rule of a 3λ channel for long-channel behavior). In terms of the choice of channel material, the term ϵ_{body} plays a minor role while d_{body} strongly affects the screening length—it is this influence of a small d_{body} that gives SWCNTs (typically 1–2.5 nm) a distinct advantage over semiconductor nanowires (typically 10–100 nm) for aggressively scaled devices. Another important observation from Fig. 2 is that the oxide thickness has a less significant impact on λ in the SG geometry than in the BG geometry. Also, the benefit to λ of using high- κ dielectrics in the SG geometry diminishes as ϵ_{ox} rises above approximately 10.

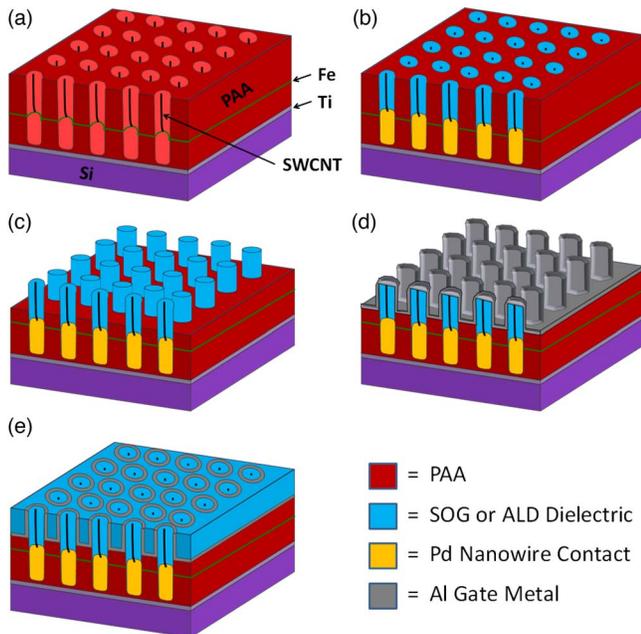


FIG. 3. (Color online) Schematic process flow for fabricating SG v-SWCNTs. The template is shown after (a) v-SWCNTs synthesis, (b) Pd nanowire electrodeposition, SOG application and ion bombardment etchback, (c) selective etchback of PAA, (d) sputtering of Al gate metal, and (e) SOG application and final ion bombardment etchback. Note that these schematics are qualitative and therefore not necessarily to scale.

III. FABRICATION OF SURROUND GATES

Figure 3 illustrates the process for fabricating SGs on v-SWCNTs templated in PAA. Beginning with a thermally evaporated thin film of 100 nm Ti/100 nm Al/1 nm Fe/300 nm Al (bottom to top) on a thermally oxidized Si wafer, PAA is formed by anodizing the Al in 0.3M oxalic acid at 40 V relative to a counter Pt gauze electrode at a constant temperature of 5 °C.¹¹ The resulting template contains pores with an average diameter of 20 nm at a spacing of approximately 100 nm. The v-SWCNTs are synthesized in a microwave plasma chemical vapor deposition (MPCVD) system flowing 50 SCCM (SCCM denotes cubic centimeter per minute at STP) hydrogen and 10 SCCM methane gases with a 300 W plasma at 10 torr and a substrate temperature of 900 °C as monitored from an embedded thermocouple.¹⁰ The SWCNTs grow vertically from the Fe layer embedded in the PAA, and extend beyond [see Fig. 3(a)] the top of the PAA, at a yield of no more than one SWCNT per pore.¹⁰ The percentage of pores that contain a SWCNT has not been determined, but this characteristic can be adjusted by varying the MPCVD growth conditions and can range from a few percent to more than 50%.¹⁶ Characterization of the nanotubes from this growth process has been reported elsewhere and revealed distinct single-walled nature in both Raman and transmission electron microscope analyses.^{10,12} After v-SWCNT growth, Pd is electrodeposited into the PAA to form Pd nanowire bottom contacts to the nanotubes.^{11,12}

To achieve the structure shown in Fig. 3(b), a silicate spin-on glass (SOG) from Honeywell (Product No. 214) is first spin coated onto the samples at 6000 rpm for 30 s. The

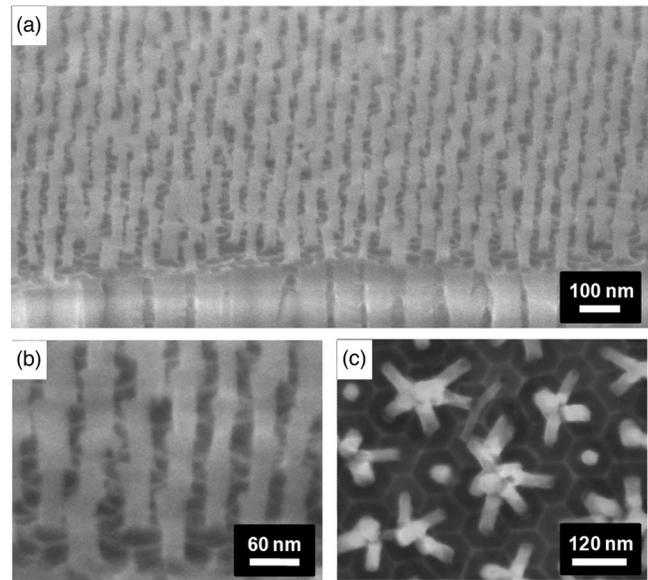


FIG. 4. (a) and (b) are tilted cross-sectional SEM images of dielectric pillars in a highly ordered hexagonal arrangement after selectively etching back the PAA; v-SWCNTs are within the dielectric pillars. (c) is a top-view SEM image showing the agglomeration of SOG pillars that occurs when the aspect ratio becomes too large.

SOG is then cured on hotplates of 80, 150, and 250 °C for 1 min each. A final cure of the SOG is performed at 450 °C for 1 h in a quartz tube furnace with a nitrogen ambient. Next, the SOG is etched back to the PAA surface to expose the PAA and the v-SWCNT tips using an Ar ion bombardment in an inductively coupled plasma reactive ion etcher. The Ar ion bombardment was carried out with 60 SCCM Ar, 300 W coil power, and 800 W platen power at 0.5 mtorr for 90 s. Previous work discusses the use of this ion etch to control the length of the v-SWCNTs to the sub-100-nm regime.¹³ It is important to note that while SOG is used for demonstration in this work, atomic layer deposition (ALD) of a high- κ dielectric is another viable method for filling the pores and supporting the v-SWCNTs.¹⁷ Work toward the use of ALD for this process is currently underway.

One advantage of having each v-SWCNT supported in its own channel with the SOG dielectric is that the PAA can now be selectively etched back to expose these rigid dielectric pillars, which serve to template the SG formation. As mentioned previously, SWCNTs are not rigid so it is more difficult to realize a SG structure around a SWCNT than for a semiconductor nanowire. In a solution of chromic acid at 65 °C, the PAA is etched back at a rate of approximately 7 nm/min. This slow etch rate provides the ability to accurately define the portion of the source-to-drain channel length that is to be gated for the device. Once the PAA has been etched back [see Fig. 3(c) and Fig. 4], the Al gate metal is sputtered in a dc sputtering system with an Ar gas support at 75 W and 10 mtorr for 10 min. The result is a conformal Al thin film on the SOG/v-SWCNT pillars of approximately 20 nm (the Al film thickness varies from the PAA surface to the top of the pillars due to shadowing effects, but the film

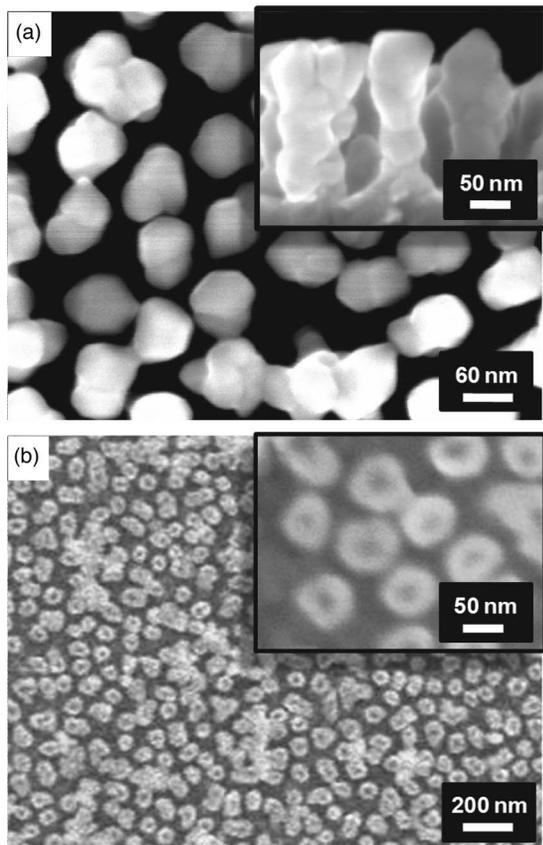


FIG. 5. (a) Top-view SEM image of the dielectric pillars after sputtering of Al gate metal; the inset shows cross section of the pillars. (b) Top-view SEM image of the final SG on v-SWCNTs with the metal coated pillars supported in SOG—each bright ring is the Al gate metal with a dielectric pillar within the ring surrounding a v-SWCNT.

appears to be continuous) as shown in the field-emission scanning electron microscope (SEM) images in Fig. 5(a).

The final step to completing the SG v-SWCNTs begins with applying another SOG layer using the same process employed to fill the pores initially. This final SOG layer acts as a support for the SG pillars and allows the final gated channel length to be defined. After application and curing, the SOG is etched back using the same Ar ion bombardment process described above. This time, the ion etch is continued until the cylindrical Al gate metal is exposed, as shown in Fig. 5(b), at which time the v-SWCNT tips also become exposed. The etch time for this process was 50 s, but continuing the etch past this time allows for further scaling of the SG v-SWCNT channel at a rate of approximately 60 nm/min, similar to the previously reported demonstration of controlling the length of the v-SWCNTs using this etch.¹³

IV. RESULTS AND DISCUSSION

Results of selectively etching back the PAA to expose the v-SWCNTs wrapped in the rigid dielectric pillars are given in the SEM images of Fig. 4. Note that the pillars are the same diameter as the initial PAA pores, 20–25 nm with an inner-pore spacing of 100 nm in the current experiment. A limit exists as to how far these pillars can be exposed be-

cause as their aspect ratio increases, attractive van der Waals forces will cause adjacent pillars to agglomerate. The adhesion force (F_{ad}) between two adjacent SOG pillars is calculated according to Derjaguin-Muller-Toporov¹⁸ theory as

$$F_{ad} = 2\pi RW_{ad}, \quad (3)$$

where R is the radius of the pillar and W_{ad} is the work of adhesion of the SOG. The elastic force generated by bending a pillar of stiffness k_b ($k_b = 3\pi R^4 E / 4l^3$) over a displacement δ is

$$F_{el} = \frac{3\pi R^4 E}{4l^3} \delta, \quad (4)$$

where l is the length of the pillars and E is Young's modulus of the SOG.

In order to prevent the pillars from adhering to each other, the elastic force must be greater than the adhesion force. Solving the inequality between Eqs. (3) and (4), the maximum length of the pillars before they agglomerate is

$$l \leq \left(\frac{3SR^3 E}{16W_{ad}} \right)^{1/3}, \quad (5)$$

where $S = 2\delta$ is the spacing between the pillars. Assuming Young's modulus of 20 GPa (approximately one-third that of SiO_2)¹⁹ and work of adhesion of 0.12 N/m,²⁰ the maximum pillar length ($R = 10$ nm, $S = 100$ nm) is 146 nm. It should be noted that the calculated length is for SOG pillars in air; however, during the drying of the SOG pillars after length definition in the chromic acid, capillary forces will increase the adhesion force between pillars,²¹ and this effect will cause agglomeration at somewhat shorter lengths. Experimentally, we observed agglomeration of the pillars to occur when they reached approximately 110 nm in length, as shown in Fig. 4(c).

The dimensions of the PAA templates in this study would yield devices with a d_{ox} of ≈ 9 –12 nm and an ϵ_{ox} of ≈ 3.9 (the SOG is a silicate with a dielectric constant similar to SiO_2). Also, the SWCNTs have a diameter of approximately 1–2 nm and have been shown to have ϵ_{body} values in the range of 20–30.²² Therefore, this SG device geometry would yield a screening length of $\lambda \approx 3$ nm, which is one-fourth of the λ achieved from the same parameters using a BG geometry. Replacement of the SOG with an ALD deposited high- κ dielectric would cut the screening length to 1.5 nm for the SG and improve the switching of the resulting FET. The PAA pore diameter and spacing can also be scaled to smaller dimensions by anodizing at lower voltages or in a different electrolyte (e.g., sulfuric acid),¹¹ which would subsequently decrease d_{ox} .

The top-down nature of this vertical process for fabricating SGs on SWCNTs is highly advantageous in the context of manufacturing SWCNT-FETs. The carbon nanotubes are grown, gate dielectric applied, metal deposited, and channel length defined across all devices on a chip using inexpensive and high-throughput processes compared to the more commonly used postsynthesis dispersion of SWCNTs combined with electron-beam lithography.^{2,5,23–26}

At two points of this fabrication process an Ar ion bombardment etch was employed to planarize the SOG-filled template [see Figs. 3(b) and 3(e)]. Initially, reactive ion etching using fluorine-containing gases was attempted; however, the fluorine content proved to reactively etch the SWCNTs, completely removing them from the template. Therefore, this inert gas mechanical etch was developed to minimize the reactive etching component, while still resulting in a relatively planar surface. Although each material (alumina, SOG, Al, and SWCNT) may etch at a slightly different rate, the variability in etch rate was less than approximately 10 nm/min, as observed by the thickness uniformity of the templates following many etching trials. A potential shortcoming to the bombardment etch is the resulting formation of dangling bonds on the tips of the v-SWCNTs; dangling bonds could adversely impact the carrier transport between the nanotube and a top contact metal. A more detailed study of the transport properties between the v-SWCNTs and top/bottom metal contacts has recently been reported.¹³

The channel length of these SG v-SWCNTs was controlled using two process steps: (1) the etch back of the PAA to expose the dielectric pillars, and (2) the final etch of the SOG filler to expose the v-SWCNT tips. For the samples fabricated in this work, the final SG channel length had a maximum variability of ± 15 nm as measured using cross-sectional SEM images. However, it is important to note that only one of the PAA templates used in this study had highly ordered pores, which can be achieved in thin films using additional processes.^{13,27,28} With ordered pores, the uniformity of the etching will improve, thus reducing the variation in channel length across a sample. Furthermore, improvement of the initial Al film surface roughness and the dielectric layer uniformity (SOG in this case) can also increase the uniformity of channel length.

Another advantage of these SG v-SWCNTs for FETs is that they lend themselves to the facile fabrication of multinanotube devices. The current-carrying capacity for many devices based on nanomaterials can be impressively high for their nanoscale dimensions; yet, in spite of such capacity, single nanowires or nanotubes are not able to produce the milliamps of current necessary for driving on-chip interconnects.²⁹ This shortcoming in drive current means that practical realization of nanomaterial-enabled nanoelectronics will require multinanotube FETs. In these modified PAA templates, v-SWCNTs grow at a yield of no more than one per pore and the pores can be fabricated in highly ordered arrays. Such arrays allow for the definition of the desired number of channels for a FET simply by defining an appropriately sized top contact to the surface shown in Fig. 5(b) that will encompass a certain number of pores and thus v-SWCNTs. Note that a short from the top contact to the gate metal can be avoided by oxidizing the Al to form alumina to the desired depth, thus creating an insulating barrier between the two metallizations. The final device structure would contain a single underlap between the gate and source. Recent simula-

tions have proven this underlap to be advantageous for obtaining *n*- and *p*-type FETs simply by changing the polarity of the drain bias.³⁰

In the context of multinanotube FETs, the templated v-SWCNTs with SGs also reduces charge screening among nanotubes compared to planar SWCNT devices.^{31,32} When SWCNTs are packed close together, a capacitive coupling develops between them that causes a screening of the gate charge and thus a degradation of the current per nanotube. Multinanotube SWCNT FETs that have been demonstrated to date all suffer from inconsistent spacing between the nanotubes and charge-screening effects from their close proximity to each other.^{25,33} In the PAA template, each v-SWCNT is 100 nm from its nearest neighbors and is individually coated in the dielectric and wrapped in the gate metal, thus allowing each channel to feel the same gate potential in a multinanotube FET.

It is important to note that the v-SWCNTs in the PAA still contain a mixture of metallic and semiconducting types. However, recent work using the same growth procedure shows a strong selectivity toward semiconducting nanotubes (95% of characterized nanotubes were semiconducting).¹³ Also, metallic nanotubes can be selectively removed by turning the semiconducting nanotubes off with the gate bias and sweeping a high bias on the metallic nanotubes to burn them out.³⁴ Ultimately, when each multinanotube device contains a certain number of SG v-SWCNT channels, the statistical distribution of their band gap energies should be comparable from device to device,³⁵ creating *I-V* characteristics within the same operating range as compared to the variation seen when testing many single nanotube devices.²³

V. CONCLUSION

In comparison to BG devices, SG SWCNT devices offer several advantages, including the ability to scale channel length more aggressively without incurring degrading short-channel effects. Using v-SWCNTs in a PAA template, fabrication of SGs on an array of channels was demonstrated. The final channel length for the vertical SG nanotubes studied herein showed a variability of ± 15 nm, which can be improved by utilizing highly ordered PAA templates. Overall, the v-SWCNTs-in-PAA structure provides a platform for using top-down processes in the formation of a SG dielectric and metal as well as in defining the channel length for all devices across an entire sample. Integration of these v-SWCNTs with SGs into devices should provide 1D multinanotube FETs with the maximum channel scaling ability together with fabrication that can be scaled to a practical manufacturing level.

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