LETTERS
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Length scaling of carbon nanotube transistors

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Carbon nanotube field-effect transistors are strong candidates in replacing or supplementing silicon technology. Although theoretical studies have projected that nanotube transistors will perform well at nanoscale device dimensions[1–4], most experimental studies have been carried out on devices that are about ten times larger than current silicon transistors[5–7]. Here, we show that nanotube transistors maintain their performance as their channel length is scaled from 3 μm to 15 nm, with an absence of so-called short-channel effects. The 15-nm device has the shortest channel length and highest room-temperature conductance ($0.7G_0$) and transconductance (40 μS) of any nanotube transistor reported to date. We also show the first experimental evidence that nanotube device performance depends significantly on contact length, in contrast to some previous reports[8–10]. Data for both channel and contact length scaling were gathered by constructing multiple devices on a single carbon nanotube. Finally, we demonstrate the performance of a nanotube transistor with channel and contact lengths of 20 nm, an on-current of 10 μA, an on/off current ratio of 1×10^5, and peak transconductance of 20 μS. These results provide an experimental forecast for carbon nanotube device performance at dimensions suitable for future transistor technology nodes.

When considering scaling the dimensions of a transistor to increase packing density on a chip, there are two lengths that are most critical: the channel length (L_{ch}, distance between source and drain) and the contact length (L_c, length of source/drain). If carbon nanotube (CNT) transistors are to be applied in future technology, all device performance limitations associated with the scaling of these dimensions must be known. The smallest channel length reported for a nanotube transistor is 18 nm, with an equivalent oxide thickness of 12 nm; this yielded poor electrostatics and thus short-channel effects[6]. Other reports of small nanotube devices only scale L_{ch} to $38-50$ nm (refs 5, 7, 11). Furthermore, the few studies to date that have included contact length scaling have focused on large-diameter multiwalled nanotubes with micrometre-scale contacts[12,13], which do not relate directly to small single-walled nanotubes with nanometre-scale contacts. Although there are hundreds of reports involving nanotube transistors, comparing the data from different studies would not create an accurate picture due to device geometry and nanotube diameter (d_{CNT}) variations (the bandgap, E_g, of a nanotube is inversely proportional to its diameter)[14].

In this study, we fabricated sets of nanotube transistors with different channel or contact lengths, with each set located on a single, unique nanotube so that the direct effects of scaling of these critical dimensions could be observed without having to take into account variations in diameter or geometry. Aligned single-walled nanotubes grown on quartz substrates[15] were transferred to a silicon substrate[16] with preformed palladium local bottom gates (LBG) capped with 10 nm HfO_2 (equivalent oxide thickness of 2 nm) (Supplementary Figs S1–3). The schematic and corresponding scanning electron microscope (SEM) image in Fig. 1a show a set of LBG transistors of various channel lengths on the same nanotube. The characteristics presented in Fig. 1b,c are taken from devices spanning two orders of magnitude in L_{ch}, with the 15-nm device being the shortest channel nanotube transistor investigated to date.

The aggressive channel length scaling yielded improvement in on-state performance, while maintaining consistent off-state attributes, including a steady inverse subthreshold slope (*SS*) and threshold voltage (V_{th}). There was no observed drain-induced barrier lowering in the devices, and although the I_d-V_{LBG} curves were occasionally observed to shift slightly, there was no consistency to the shifting, no dependence on V_{ds}, and it occurred for all transistors, including those with long channels (thus, it was interpreted as being an effect of charges in the oxide rather than a loss of gate control over the channel). No short-channel effects were therefore observed, even in the 15-nm device. The superb performance of these devices was achieved in spite of the relatively small d_{CNT} ($1.1 < d_{CNT} < 1.3$ nm, as determined from atomic force microscopy) compared with previously reported, high-performance nanotube transistors[5,7] (smaller d_{CNT} (larger E_g) yields larger Schottky barriers, usually hampering the on-state[17]). Such impressive on- and off-state performance is a result of the superior electrostatics of the LBG geometry[11]. With the gate beneath the nanotube, there is no restriction to the gate dielectric thickness as exists in top gate geometries, where the dielectric must be thick enough to be built up around the inert nanotube[18]. Although it has proven difficult to implement effectively, incorporating a completely wrap-around gate would yield the optimum electrostatics for nanotube devices[19,20], providing maximum channel scalability.

The $I_d - V_{ds}$ characteristics in Fig. 2a show how L_{ch} scaling affects the low-field slope and saturation current at the same gate overdrive ($V_{LBG} - V_{th}$). Note how similar the curves are for the 15- and 40-nm L_{ch} devices, indicating that at low fields scattering in the channel plays a very minor role in device performance. These ultrasmall-L_{ch} devices exhibit room-temperature, low-field resistances of $9-11$ kΩ ($110-91$ μS), which is closer to the quantum limit ($R_Q = 1/G_0 = h/4e^2 \approx 6.5$ kΩ) than has been reported to date. Furthermore, devices of different lengths were fabricated on a metallic nanotube (Fig. 2b) for comparison; these exhibited resistances down to 6.6 kΩ, which is the lowest observed for any single nanotube.

One of the most useful tools for extracting information from L_{ch} scaling is a transfer length model[21,22] plot of the total resistance (R_{tot}) versus L_{ch}. The R_{tot} values for all devices reported here had a nontrivial contribution from the small metal contact leads, which was accounted for by measuring the resistance in similar metal line structures (Supplementary Fig. S5). After taking into account this contribution, R_{tot} from several sets of devices was plotted in Fig. 2c, with each set having been taken for a different nanotube. The total resistance is a series combination of the channel resistance (which is the result of reduced

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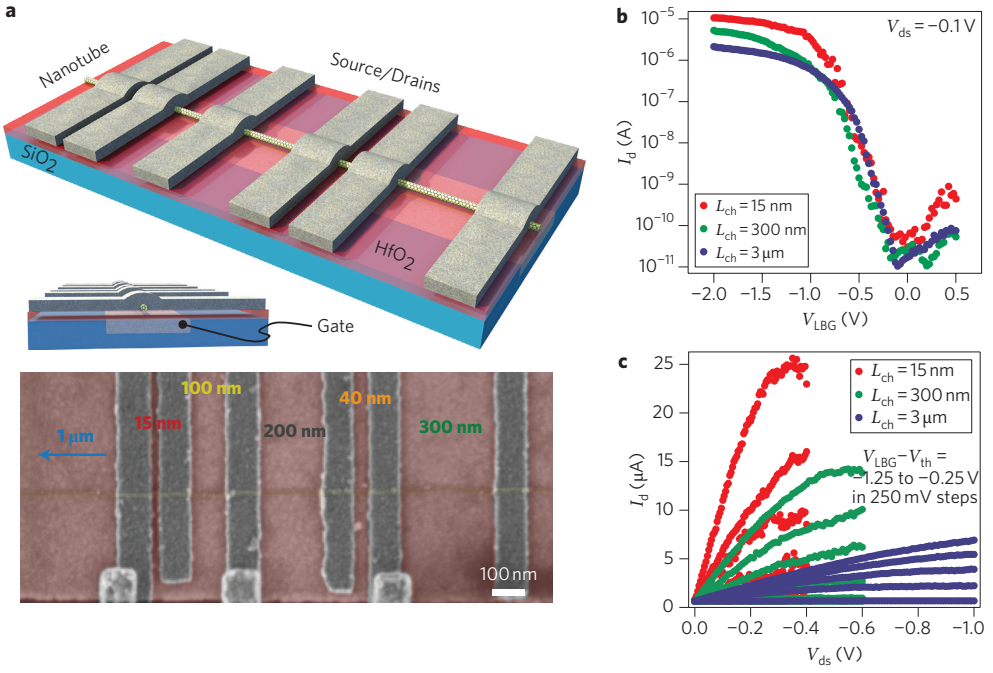

Figure 1 | Effects of channel length scaling on nanotube transistor performance. a, Schematic of a set of transistors on the same nanotube with L_{ch} ranging from 15 nm to 1 μm. The nanotube rests on a local bottom gate (LBG) that is covered with 10 nm HfO_2 (equivalent oxide thickness, ~2 nm). A representative, false-coloured SEM image is also shown. **b**, Subthreshold $I_d - V_{LBG}$ data from $L_{ch} \approx 15$ nm, 300 nm and 3 μm devices, showing the consistency of V_{th} and SS when scaling channel length over two orders of magnitude. **c**, Output $I_d - V_{ds}$ characteristics (plotted at the same gate overdrive) for the same devices as in **b**, demonstrating dramatic improvement in on-state performance when L_{ch} is aggressively scaled. The peak transconductance for the 15-nm device is 40 μS. For all extremely scaled L_{ch} devices, drain–source bias much greater than 0.5 V caused breakdown of the nanotubes. Passivation and/or testing in vacuum could be used to protect the nanotubes at higher fields. The 15-nm channel is ballistic, meaning that the voltage is dropped entirely at the contact – nanotube interface, resulting in very high fields. All devices have approximately the same L_c of 100 nm.

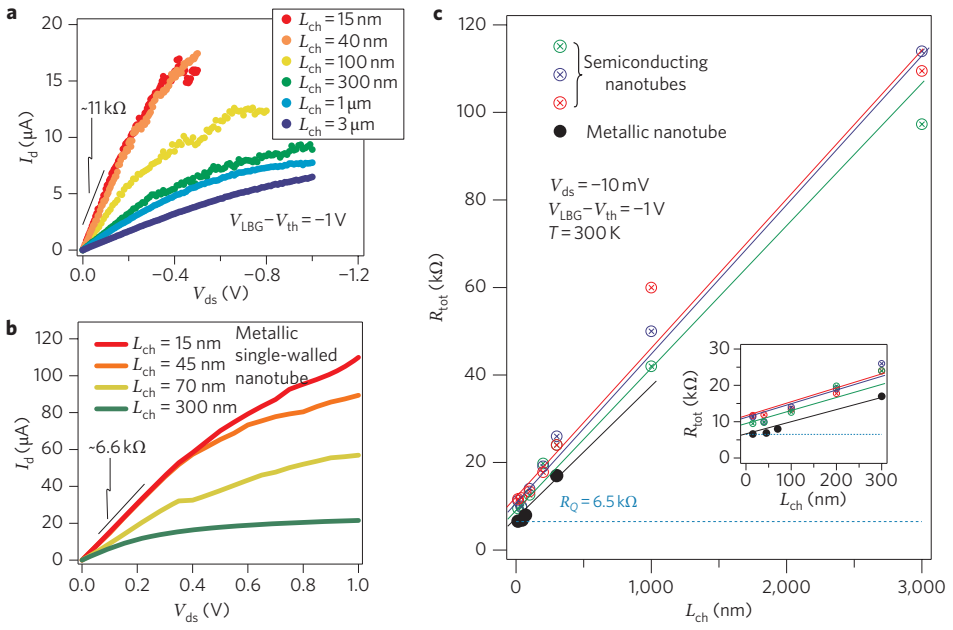

Figure 2 | Scaling to the ballistic transport regime. a, Output curves at the same gate overdrive ($V_{LBG} - V_{th}$) from a series of transistors on the same nanotube with different L_{ch}. The 40- and 15-nm devices exhibit nearly equivalent slopes, indicative of similar (nearly ballistic) channel resistances. **b**, $I_d - V_{ds}$ curves from several devices of different length on a single metallic nanotube showing less saturation for devices with lengths near the mean free path for optical phonon scattering. Note how the 45- and 15-nm devices share the same low-field slope here, just as the transistors of similar lengths do in **a**. **c**, Transfer length model plot of total resistance versus L_{ch} from three sets of transistors (each set on a different nanotube, denoted with a different colour), and from the metallic nanotube devices in **b**. All metal line resistances have been removed to obtain R_{tot}. The lines represent linear fits to the data and their average is used for extracting $2R_c$ and L_{mfp} via equation (1). The inset shows the smaller L_{ch} devices for a closer look at the R_{tot} axis intersection — the metallic nanotube fit intersects at ~6.5 kΩ = R_Q, whereas the semiconducting fits are slightly higher because of the added resistance under the contacts (for example, Schottky barriers).

transmission probability by scattering events) and the contact resistance ($2R_c$)[23]:

$$R_{tot} = \frac{h}{2e^2 M}\frac{L_{ch}}{L_{mfp}} + 2R_c \quad (1)$$

where h is Planck's constant, L_{mfp} is the mean free path for phonon scattering, and M is the number of modes in the channel ($M = 2$ for a nanotube). L_{mfp} in this case represents acoustic phonons (thermal scattering events with the lattice). Although optical or zone boundary phonons are emitted in nanotubes at high drain biases (V_{ds}) when carriers exceed the optical phonon energy (0.16 eV)[24], they can be disregarded at small V_{ds}, leaving just acoustic phonons (see Supplementary Information). As seen from the linear fits applied in Fig. 2c, the R_{tot} data follow the trend in equation (1). The slope of the linear fits is related to $1/L_{mfp}$, resulting in a consistent L_{mfp} of ~200 nm, which is in close agreement with other reports[21,24,25].

The contact resistance is extracted from the intercept on the R_{tot} axis in the plot of Fig. 2c, and comprises the quantum resistance ($R_Q = 6.5\ k\Omega$ for a nanotube)[23] and the resistance from under the contacts ($2R_{uc}$), as shown in equation (2). $2R_{uc}$ is a generalization that includes resistance from Schottky barriers and any other resistance from interfaces or transport in the contact metal-covered nanotube. Different values of d_{CNT} result in varying E_g, thus affecting $2R_{uc}$ due to changes in such parameters as Schottky barrier heights[17] and nanotube curvature (which affect coupling between the metal and nanotube, and so on), whereas R_Q remains constant. However, in spite of the variation in d_{CNT}, the distribution of $2R_c$ in the present devices is very tight (see Fig. 2c inset), which is attributed to good electrostatics allowing for thin, nearly transparent Schottky barriers and a relatively narrow d_{CNT} distribution (Supplementary Fig. S4).

Contact length scaling was studied in the same manner as L_{ch} scaling, with multiple devices located on the same nanotube (Fig. 3a). The results show that L_c scaling affects the on-state (Fig. 3c) far more dramatically than the off-state (Fig. 3b) of a device. Plotting the $I_d - V_{ds}$ curves at the same gate overdrive (Fig. 3c) allows the increase in R_{tot} to be clearly visible as L_c is reduced. This increase in resistance causes the transconductance (g_m) to reduce with L_c, as shown in the inset of Fig. 3b. Some studies have suggested that transport between a metal and a nanotube occurs only at the contact edge[8–10], with no length dependence, or that sharp needle-like contacts are ideal[26,27]; others have shown that carriers propagate in nanotubes tens of nanometres under the metal contacts[28]. These differing conclusions were drawn based on devices with $L_c > 100$ nm. The present results are the first to clearly demonstrate the length dependence of transport at metal–nanotube contacts below 100 nm.

Accounting for the small contributions of channel resistance ($L_{ch} \approx 40$ nm) and metal line resistance in the L_c scaled devices leaves just $2R_c$, which is plotted versus L_c in Fig. 4a. It was shown, above, that $2R_{uc}$ has minimal dependence on d_{CNT} in the present devices. For the following analysis, we therefore use the average of the data from the transfer length model plot to extract a specific contact resistivity (ρ_c) that can be applied to the L_c scaling data from other nanotubes. For this approach, $2R_c$ is expanded as[22,29]

$$2R_c = R_Q + 2R_{uc} = R_Q + \frac{2\rho_c}{L_c d_{CNT}} \quad (2)$$

where d_{CNT} is the average for the nanotube source (1.2 nm). Note that ρ_c differs from conventional contact resistivity because it is calculated based on partial contact resistance. Equation (2) relies on L_c being smaller than the transfer length (L_T), which is the length at which the potential drops to $1/e$ of its value. L_T is traditionally extracted from the transfer length model plot ($2L_T$ is determined as the point where the extrapolated line intercepts the L_{ch} axis),

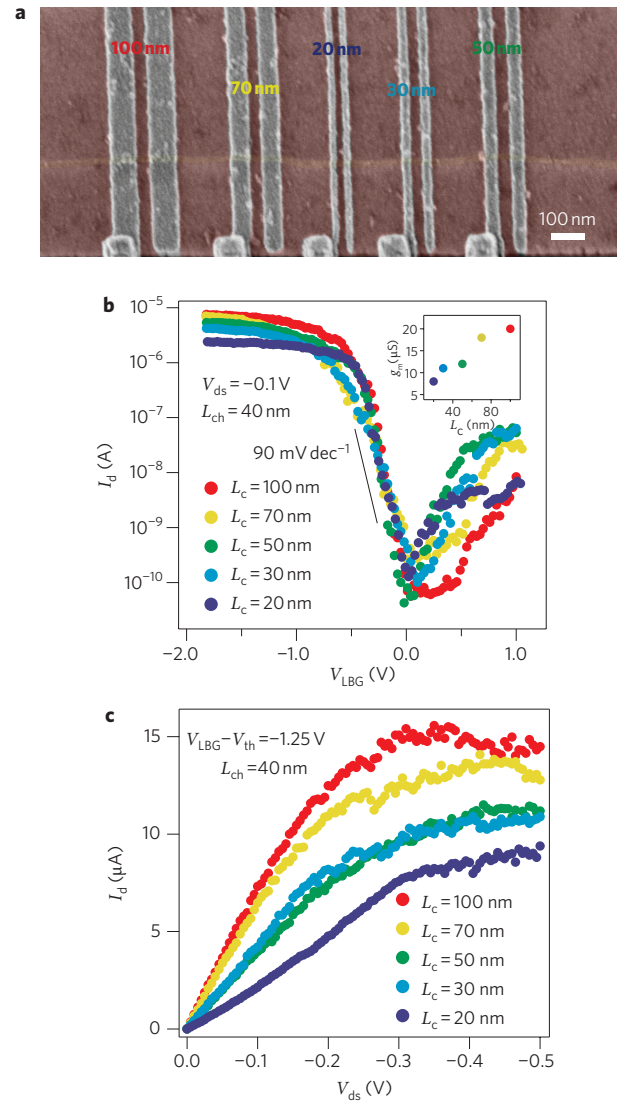

Figure 3 | Effects of contact length scaling on nanotube transistor performance. a, False-coloured SEM image of a set of transistors on the same nanotube with different L_c ranging from 100 nm to 20 nm. **b**, Subthreshold $I_d - V_{LBG}$ data from a set of devices, showing the consistency of V_{th} and SS when aggressively scaling the contact length. Inset shows the dependence of g_m on L_c. **c**, Output $I_d - V_{ds}$ characteristics (plotted at the same gate overdrive) for the same devices as in **b**, demonstrating how the on-state degrades with decreasing L_c. All devices have approximately the same L_{ch} of ~40 nm.

with the assumption that transport in the nanotube is equivalent in the channel and under the contact metal, a condition that cannot be verified at this stage. The true L_T in these devices may therefore be slightly smaller than the extracted value of 200 nm; however, with $L_c \approx 100$ nm for the transfer length model devices, equation (2) remains a reasonable approximation and yields a ρ_c of 346 kΩ nm^2. With this ρ_c, an extremely good fit is acquired for data obtained from three different sets of L_c scaled devices (each set from a different nanotube), accurately tracing the dependence of $2R_c$ on L_c (Fig. 4a). Furthermore, combining equations (1) and (2) gives the complete scaling picture for these nanotube transistors (plotted in Fig. 4b). Note that the Fig. 4b plot quantitatively relies on parameters unique to this particular device geometry, but the trend should be consistent for all nanotube transistor geometries.

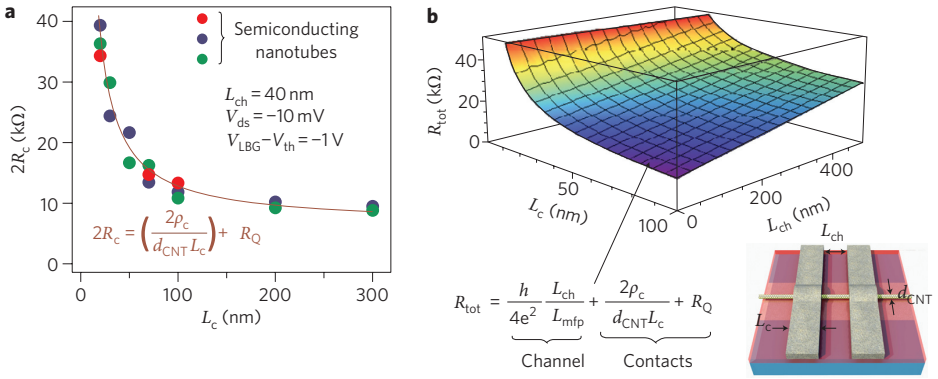

Figure 4 | $2R_c$ versus L_c trend and the complete scaling picture. a, Plot of $2R_c$ versus the contact length from several sets of transistors, with each set on a different nanotube (each colour represents a set of devices on the same nanotube). The inset expression for $2R_c$ was used to generate the curve fit with ρ_c extracted from the averaged data in the transfer length model plot (Fig. 2c). **b**, R_{tot} dependence on the two scaled lengths, L_c and L_{ch}, according to the equation shown, with L_{mfp} taken from the transfer length model plot (together with ρ_c). Note that this plot relies quantitatively on parameters unique to this particular device geometry, but the trend should be consistent for all nanotube transistor geometries. The schematic illustrates the relevant dimensions.

There are some theoretical models that support the L_c dependence of R_{tot}, suggesting that the metal − nanotube coupling relies on L_c and influences the amount of carrier reflection at the contacts, thus affecting the contact resistance[30,31]. Unfortunately, although these models consider carrier injection between the metal and nanotube, they do not provide information regarding transport in the portion of the nanotube that is covered by the metal contact. Greater elucidation of transport in metal-coated nanotubes is needed to further examine the components of ρ_c and its potential dependence on other parameters, such as L_c. At this stage, ρ_c (Fig. 4) is an excellent approximation that encompasses both the metal − nanotube injection and the metal-coated nanotube transport resistances to provide a fit to the present data; however, we are not suggesting that this represents the final physics at the contacts, as extensive, further investigation is necessary.

A final demonstration of the operation of scaled nanotube transistors is shown in Fig. 5, in which both the channel and contact lengths have been aggressively scaled ($L_{ch} \approx L_c \approx 20$ nm). This is the smallest nanotube transistor reported to date, and it performs very well, in spite of such tiny critical dimensions. An on-current of 10 μA is obtained at only −0.5 V of drain bias, and the off-state is free of short-channel effects with a very stable *SS* of ~85 mV dec^{-1}—a superb *SS* for a Schottky barrier device. Performance at these lengths can be improved further by incorporating thinner dielectrics. Additionally, the noise in the characteristics, which is related to the small number of carriers in the channel, can be reduced by incorporating several nanotubes in parallel into the channel.

In summary, this Letter has provided the first experimental evidence of the effects of aggressive channel and contact length scaling in nanotube transistors. A wide range of lengths were studied (15 nm $< L_{ch} <$ 3 μm and 20 nm $< L_c <$ 300 nm) by fabricating sets of devices with different dimensions along the same nanotube. Results showed that L_{ch} can be scaled down to 15 nm without incurring short-channel effects, yet achieving saturated on-currents of up to 25 μA for a single nanotube at $V_{ds} = -0.4$ V and $g_m \approx 40$ μS. The first evidence of contact resistance dependence on contact length has been provided, and a reasonable fit to data from three different nanotubes has been obtained. The performance costs of L_c scaling must be taken into account when considering nanotube transistors for a future technology. It is clear that there will be a trade-off between extremely scaled contacts and the best performing devices (high I_{on} and g_m). With a final demonstration of the smallest device to date, this study has provided evidence that, in spite of the cost of L_c scaling, nanotube transistors can continue to offer impressive performance at dimensions that are suitable for integration through the next decade of the technology roadmap.

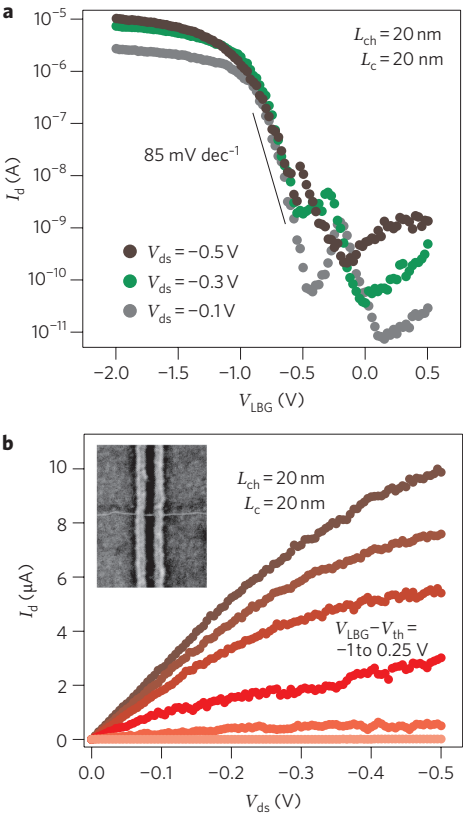

Figure 5 | Extremely scaled nanotube transistor. a, Subthreshold characteristics from the smallest nanotube transistor to date, with $L_{ch} \approx L_c \approx$ 20 nm. The diameter of the nanotube is between 1.0 and 1.2 nm, as determined by atomic force microscope measurements. **b**, Output characteristics from the same device as in **a**, exhibiting up to 10 μA of on-current at $V_{ds} = -0.5$ V with $g_m \approx 20$ μS.

Methods

Fabrication of local bottom gates. On silicon substrates with 1 μm of thermal SiO_2, 1-μm-wide LBGs were patterned into poly(methyl methacrylate) (PMMA) using electron-beam lithography. The SiO_2 was then reactive ion etched in a mixture of CHF_3 and O_2 at 100 W for 3 min to remove ~40 nm, followed by a 10 s etch in 9:1

buffered oxide etchant to remove an additional 10 nm and provide a slight undercut of the PMMA. Electron-beam evaporation was then used to sequentially deposit 10 nm titanium and 40 nm palladium, which, after lift-off in acetone at 80 °C, created palladium local bottom gates that were nearly planar with the surrounding SiO_2. Atomic-layer deposition was then used to deposit 10 nm HfO_2 at 125 °C.

Growth and transfer of aligned nanotubes. Quartz substrates were annealed overnight in air at 900 °C, and subsequently coated with a resist containing a suspension of iron catalyst particles[15]. The resist was patterned into catalyst strips 10 μm wide and 50 μm apart using optical lithography. Single-walled carbon nanotubes were grown from the catalyst particles in a 2-inch-diameter tube furnace at 900 °C for 10 min by running forming gas (95% argon/5% hydrogen) through an ethanol bubbler chilled to 0 °C, yielding approximately one nanotube per micrometre. The aligned, single-walled nanotubes were transferred to the LBG substrates by evaporating 100-nm gold onto the quartz and then applying a piece of thermal tape (RevAlpha 3198M) to the surface. The thermal tape was then gently peeled from the quartz, taking with it the gold-coated nanotubes, and deposited on the receiving substrate. Brief baking on a 130 °C hotplate deactivated the thermal tape, thereby removing it. A 5-min reactive ion etch in argon plasma cleaned the gold surface, followed by a 1-min wet etch in Transene Gold Etchant TFA to remove the gold.

Identification of semiconducting nanotubes and device fabrication. Palladium electrodes separated by 3 μm and crossing the LBGs were used to quickly locate single, semiconducting nanotubes by testing each site in a semi-automated probe station. Sets of devices were fabricated on the 3-μm-long semiconducting nanotubes by patterning source/drain contacts into thin PMMA (A2, ~40-nm thick) using electron-beam lithography and then depositing 20 nm of palladium followed by lift-off in 80 °C acetone. Electrical tests on the nanotube transistors were performed in air and at room temperature, with no further passivation or annealing treatments.

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Author contributions

A.D.F. conceived, designed and performed the experiments. A.D.F. and Z.C. analysed the data and interpreted the results. A.D.F. wrote the paper, with comments by Z.C.

Additional information

The authors declare no competing financial interests. Supplementary information accompanies this paper at www.nature.com/naturenanotechnology. Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to A.D.F.