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Carbon Nanotube Complementary Wrap-Gate Transistors

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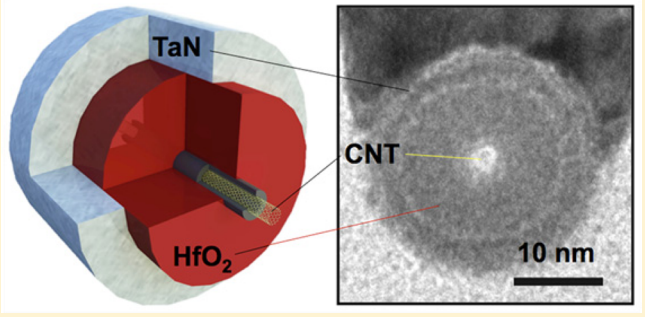
Supporting Information

ABSTRACT: Among the challenges hindering the integration of carbon nanotube (CNT) transistors in digital technology are the lack of a scalable self-aligned gate and complementary n- and p-type devices. We report CNT transistors with self-aligned gates scaled down to 20 nm in the ideal gate-all-around geometry. Uniformity of the gate wrapping the nanotube channels is confirmed, and the process is shown not to damage the CNTs. Further, both n- and p-type transistors were realized by using the appropriate gate dielectric—HfO_2 yielded n-type and Al_2O_3 yielded p-type—with quantum simulations used to explore the impact of important device parameters on performance. These discoveries not only provide a promising platform for further research into gate-all-around CNT devices but also demonstrate that scalable digital switches with realistic technological potential can be achieved with carbon nanotubes.



KEYWORDS: *Carbon nanotube, field-effect transistor, gate-all-around, wrap-gate, complementary logic, CNTFET*

The increases in semiconductor device density up until the past decade were made possible by simple scaling rules for performance of metal−oxide−semiconductor field-effect transistors (MOSFETs).[1] These rules postulate that the proper scaling of device dimensions and supply voltage will enable performance to increase and energy-per-operation to decrease, with power density staying constant. Physical limitations stopped supply voltage scaling in the early 2000s, so the simple scaling relations no longer apply. Increasing performance now comes at the cost of increasing power consumption, causing performance to level off since the mid-2000s.[2] New device architectures continue to give incremental improvements to prolong increases in device density,[3] but these are stopgaps limited by the inability to scale operating voltage.[4] An intense search for a post-MOSFET, low-voltage device is underway in academia and industry,[5] but no comprehensive solution has been identified yet.

One candidate to replace silicon MOSFETs is the carbon nanotube (CNT) field-effect transistor (FET). These have already delivered ballistic transport,[6] simple integrated circuits,[7,8] and high performance at low voltages down to sub-10 nm channel lengths.[9] However, to compete with silicon would require several major advances, including: a gate that can be scaled and is self-aligned to the source and drain contacts, complementary (n- and p-type) devices, and process compatibility with the wiring levels that are needed to build circuits. In addition, it would be ideal to have a gate that completely surrounds the CNT channel.[10,11] Such a gate-all-around (GAA) geometry[11,12] is so advantageous and natural to the CNT that it has been used in nearly all of the theoretical studies of the operation and performance limits of CNTFETs.[13−15] Due to the complete encapsulation of the CNT, GAA protects the nanotubes from the influence of neighboring devices and stray charges known to cause variations and instability[16,17] and is compatible with successive wire level processing.

Because CNTFETs are not doping-controlled devices like traditional bulk MOSFETs, their polarity is largely determined by how carriers are injected into the CNT from the source contact. With high work function metals like Pd and Au, it is straightforward to fabricate high-performance p-type CNTFETs (p-FETs) where the metal Fermi level is very nearly aligned with the valence band. Recently, n-type CNTFETs (n-FETs) with comparable performance have been demonstrated with rare earth metals such as Sc or Y.[18,19] However, the yield of such low work function metal devices is notably lower than for p-FETs,[19] largely because these metals are readily oxidized. Other demonstrations of n-FETs rely on geometry, chemical processes, or both that are either not scalable or not uniform, although they have yielded a few high-performance devices.[20−22]

In this work, we show that complementary n- and p-FETs can be delivered in the ideal GAA geometry. The polarity is controlled by the choice of gate dielectric, with an n-FET realized by a doping effect that is attributed to a dipole layer formed at the interface between HfO_2 and an adhesion dielectric layer. Further, as required for any practical

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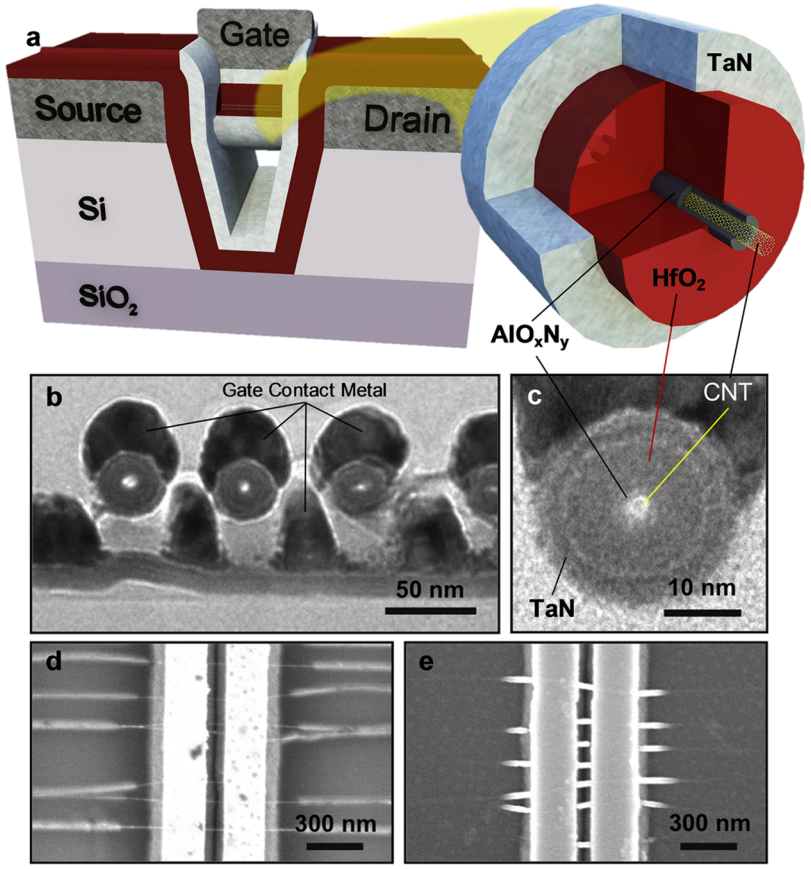

Figure 1. Carbon nanotube transistor with ideal gate-all-around geometry. (a) Cross-sectional schematic of the device illustrating how the GAA-CNT channel is suspended across the Si trench and contacted on either side by Pd source/drain (the Pd gate contact on top would also be present on either side of the GAA in the trench but is not shown here for greater clarity). Inset cutaway diagram illustrates the GAA materials in greater detail, including ~1 nm AlO_xN_y, 8 nm HfO_2, and 5 nm TaN. Cross-sectional TEM images of (b) an array of CNTs with GAA and (c) a higher magnification of a GAA with the CNT visible in the center. Top-view SEM images of an array of CNTs suspended between Pd contacts (bright vertical bars) (d) before and (e) after GAA formation. Note in d how charging causes the CNTs to look larger when they interface with the SiO_2 surface away from the contacts.

technology, the GAA in these CNTFETs is self-aligned to the source and drain contacts, and is scalable, with gate lengths down to 20 nm demonstrated. Although there are a few examples of self-aligned CNTFETs reported, they rely on device structures with either large underlaps[21,23] or extremely thin source/drain/gate contacts[24,25]—neither of which can be scaled. A self-aligned gate is one that has a consistent alignment to, or separation from, the source and drain contacts that is not controlled by lithography; further, a self-aligned gate does not overlap or excessively underlap the source/drain.

To achieve a GAA requires first suspending the nanotube channels. For this, a wet etch was adapted to a silicon-on-insulator (SOI) substrate with a (110) Si surface orientation, enabling an anisotropic wet etch of the silicon with high selectivity.[26] After the nanotubes were transferred to the SOI substrate and Pd source and drain contacts were established, the Si was etched in a KOH solution, thus suspending the nanotubes. Raman measurements were used to confirm that the CNTs were not damaged during these processes (Figure S1, Supporting Information). Atomic layer deposition (ALD) was then used to deposit a concentric adhesion layer (AlO_xN_y), gate dielectric, and gate metal (TaN) around the nanotubes (Figure 1a). A similar adhesion layer was explored previously with CNTs and graphene and found to degrade carrier transport and device switching behavior.[12,27,28] We discovered that, by annealing the AlO_xN_y adhesion layer at 300 °C in Ar prior to further dielectric deposition, the impact on device performance becomes undetectable, and the layer actually improves bottom-gated CNTFETs when used to passivate them (Figure S2, Supporting Information).

We verified that the ALD layers completely encompassed the CNTs using transmission electron microscope (TEM) imaging. The TEM images in Figure 1b and c show how the GAA layers uniformly wrap each individual nanotube, suggesting the possibility of further scaling of the dielectric thickness. Top-view scanning electron microscope (SEM) images provide another perspective of how the CNT channels are suspended after the Si etch (Figure 1d) and after the GAA formation (Figure 1e). Although the ALD provided a local TaN gate metal to complete the GAA, a final gate contact was required to electrically address the TaN layer. This final gate contact must be self-aligned to the source and drain to realize devices with minimal and consistent parasitic capacitances. Figure 2a and c shows SEM images for devices of two different gate lengths (L_g) before deposition of the gate contact. The final gate contact must selectively fill in the space between the source and drain without covering them in order to achieve self-alignment. To realize such self-alignment, the gate contact was designed with a slight source/drain overlap, relying on factors such as the depth of the trench to cause the gate contact to selectively lift-

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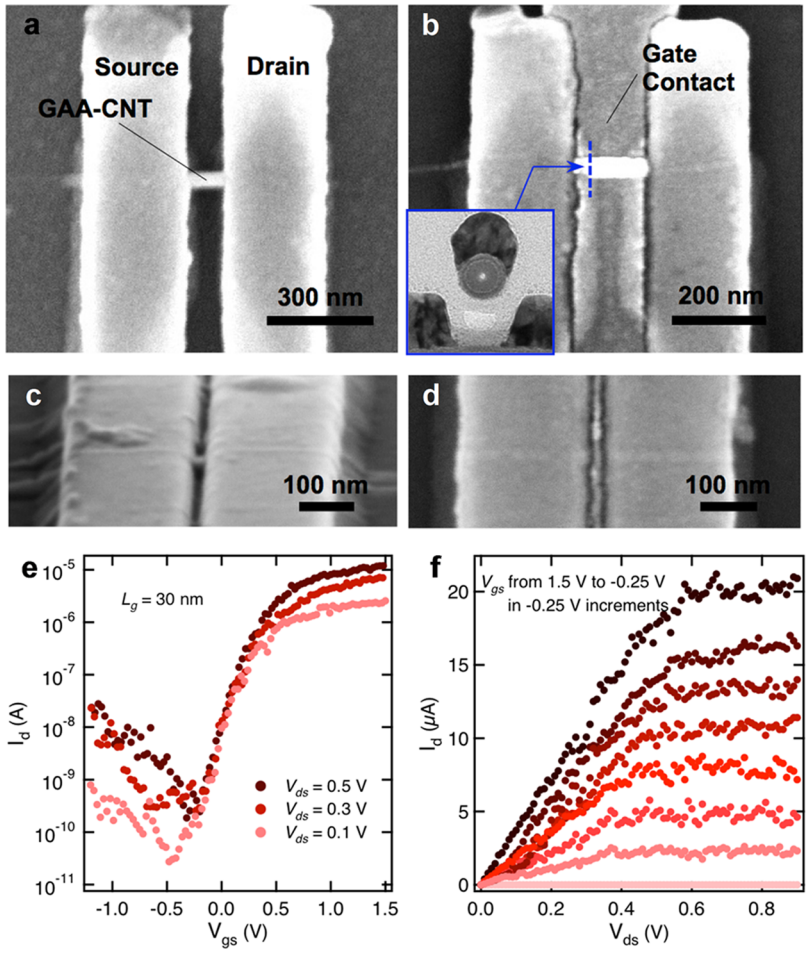

Figure 2. Self-aligned GAA including n-FET with gate length of 30 nm. SEM images of long GAA nanotube channels (a) before and (b) after the self-aligned gate contact is formed—note how the gate contact (middle electrode in b) mirrors the line edge roughness of the source/drain contacts. (c) and (d) SEM images for a ∼30 nm gate length device before and after the gate contact, respectively. (e) Subthreshold characteristics of a self-aligned GAA-CNTFET with a 1 nm AlO_xN_y/8 nm HfO_2 gate dielectric and a single CNT channel having a subthreshold swing of 99 mV/decade and on/off ratio of 10^4. (f) Output characteristics of the device showing on-state performance with strong current saturation.

off from the source/drain and remain only in the trench (Figure S3, Supporting Information). As seen in Figure 2b and d, this approach yields a gate contact that precisely mirrors the line edge roughness of the source and drain, even when L_g is scaled below 20 nm. This structure also lends itself to an alternative method for achieving reliable self-alignment using a well-established manufacturing technique, chemical mechanical planarization, by depositing a thick layer of metal such as W and then polishing the layer down to the source/drain.

Characteristics of a self-aligned GAA-CNTFET are shown in Figure 2e and f. The device exhibits superb on-state performance, with >15 μA of current at a gate overdrive ($V_{gs} - V_t$) of 1 V, where the threshold voltage, V_t is 0.25 V as determined by linear fit to, and extrapolation from, the high slope region of the transfer curve (Figure S4, Supporting Information). The off-state shows an on/off ratio >10^4 and a subthreshold swing (SS) of 99 mV/decade. Gate leakage is in the picoampere range, which is further evidence of the potential to scale the dielectric (Figure S4, Supporting Information). Hysteresis is also very low compared to bottom-gated CNTFETs (Figure S5, Supporting Information). Noise in the output characteristics results from the small number of carriers in the channel, the presence of trapped charge in the nonoptimized dielectric,[17] and tunneling through a sizable Schottky barrier for electron injection (because the device is an n-FET, as discussed below).[29] With improvement in the dielectric quality and smaller Schottky barriers (e.g., by using low work function metal contacts for the n-FET), the noise is expected to reduce considerably.

Curiously, this device is an n-FET despite having high work function Pd contacts. To determine the origin of this unexpected shift in polarity, the GAA dielectric stack was applied as a top-coating passivation layer to bottom-gated CNTFETs (Figure S6, Supporting Information). The result was a complete polarity shift from p-FETs to n-FETs, but only after deposition of the HfO_2; deposition of the AlO_xN_y layer caused degradation in device on- and off-state performance, both of which were recovered and even improved after the 300 °C anneal, and all devices remained p-type. This impact of the HfO_2 dielectric on bottom-gated CNTFETs suggests that the shift is a result of a charge dipole layer formed at the AlO_xN_y and HfO_2 interface. The mechanism for this dipole layer forming is related to the more electropositive Al metal more strongly attracting the electrons in the oxygen ions compared to the neighboring Hf metal, thus creating a dipole around the oxygen ions.[30] Owing to the sensitivity of CNTs to charge that is in close proximity, this dipole layer causes a shift in the energy bands of the nanotube, effectively doping it n-type

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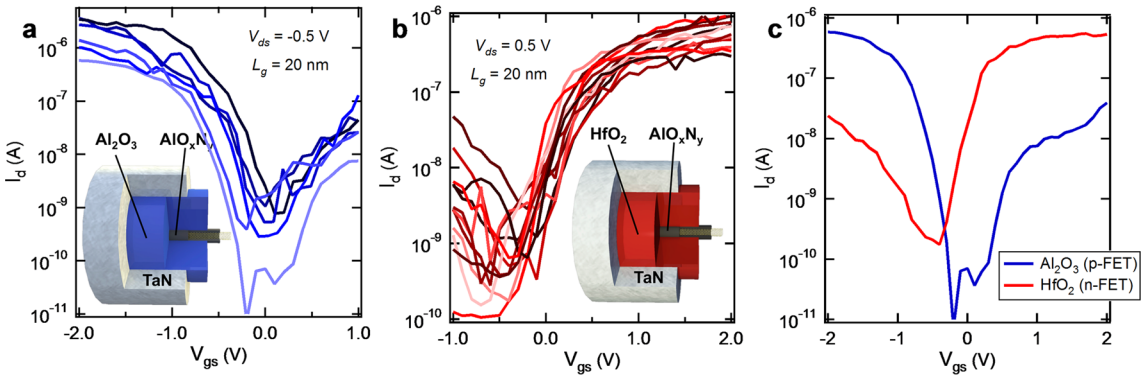

Figure 3. Complementary n- and p-type GAA-CNTFETs achieved by using different gate dielectrics. (a) Subthreshold curves from six p-FETs, each with a single CNT channel, from a chip with 1.5 nm AlO_xN_y/5 nm Al_2O_3 dielectric. The SS range for the p-FETs is 85 mV/dec to 140 mV/dec. (b) Subthreshold curves from 12 single channel n-FETs from a chip with 1.5 nm AlO_xN_y/5 nm HfO_2 dielectric. The SS range for the n-FETs is 95 mV/dec to 150 mV/dec. (c) Comparison of the characteristics of a representative p- and n-FET showing how well they work as complementary devices. All devices have a gate length of ~20 nm.

(Figure S7, Supporting Information, shows capacitance characteristics of the gate dielectric stack). A similar effect was recently observed when HfO_2 was used as the gate dielectric for CNTFETs, with the CNTs resting on SiO_2, which would create a dipole at the HfO_2/SiO_2 interface.[31,32]

The use of a gate dielectric stack that does not create a substantial dipole layer (AlO_xN_y/Al_2O_3) enabled p-FETs in this same structure. Figure 3 confirms that the polarity is completely reversed simply by changing the gate dielectric for these GAA-CNTFETs. Comparing Figure 3a and b shows that the p-FETs are indeed complementary to the n-FETs (Figure 3c). The p-FETs differ from the n-FETs in that the spacer regions (area between the TaN gate and the source/drain, consisting of AlO_xN_y/Al_2O_3 for p-FETs and AlO_xN_y/HfO_2 for n-FETs) are not impacted by a dipole layer. Because the CNTs are intrinsic semiconductors, these spacers provide a barrier to carrier transport in the p-FETs that also is not effectively modulated by the gate. As a result, the performance of the p-FETs is more variable than for the n-FETs (different CNT diameters is another source of variability for both p- and n-FETs).[16] With a thinner spacer region, or some form of effective doping of the spacers as with the n-FETs, the p-FET performance could be improved considerably.

A comparison of the performance of these GAA devices to other CNTFETs with comparable gate lengths is shown in Figure 4. For the on-state, the on-current (I_{on}) is compared at the same drain-source voltage (V_{ds}) and gate overdrive ($V_{gs} - V_t$) for all devices. As pointed out above, the spacer regions of the p-FETs are not doped in any fashion and thus contribute a series resistance that limits their on-state performance. While the spacers are effectually doped for the GAA n-FETs, the I_{on} is low for most devices because of the sizable Schottky barrier to electron injection caused by the high work function Pd contacts. Use of low work function metals will solve this additional resistance issue.

For subthreshold swing in Figure 4b, the GAA p- and n-FETs perform on par with other CNTFETs at similar gate lengths. Carrier transport through the spacer regions in the p-FETs will hamper SS considerably. The tunneling of carriers through the Schottky barrier in the n-FETs lowers their SS. In both polarity devices the presence of interface traps in the nonoptimized gate dielectrics (see Supporting Information) is another important hindrance to achieving the optimal SS. While many would expect SS to be remarkably better in these GAA devices

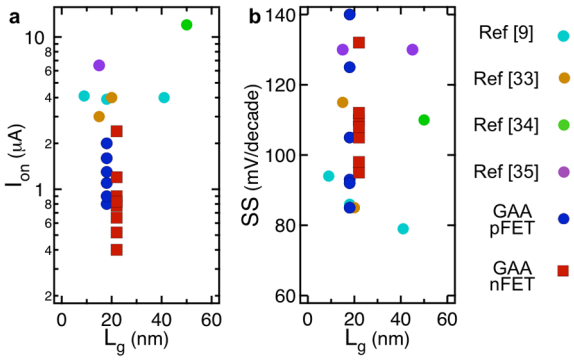

Figure 4. Comparison of the (a) on-current and (b) subthreshold swing from the GAA p- and n-FETs with the best reported CNTFETs of comparable gate lengths in the literature.[9,33−35] On-current is extracted at $|V_{ds}|$ = 0.4 V and an overdrive of $|V_{gs} - V_t|$ = 0.4 V, representative of a low operating voltage needed at sub-10 nm technology nodes. Extraction from referenced studies was approximated from reported data curves if not explicitly provided. Note that the gate length (L_g) for all GAA devices is approximately 20 nm, but the data are slightly offset (−2 nm for p-FETs and +2 nm for n-FETs) for better clarity.

because of the more ideal geometry for electrostatics, previous scaling studies have clearly shown that a simple back-gate geometry with an appropriately small equivalent oxide thickness (EOT) provides a strong enough coupling to the CNT channel to obtain excellent switching to sub-10 nm.[9] In short, all of the devices shown in Figure 4 could see improvement in SS with engineering optimization of their gate dielectric.

To confirm our understanding of the operation of these complementary GAA-CNTFETs, we performed quantum simulations of the devices using the self-consistent non-equilibrium Green's function (NEGF) formalism.[15] The p-FET was simulated using Al_2O_3 as the gate dielectric, resulting in the subthreshold curves in Figure 5a. For the n-FET, the effective doping of the nanotube was described by a doping density (N_d) applied along the CNT. The resulting characteristics in Figure 5b provide a good fit to the n-FET data for the 30 nm gate length device in Figure 2e. We can now project the impact of different variables on device performance, including spacer thickness and doping density—these are shown in Figure 5c−d. Band diagrams were also simulated to illustrate

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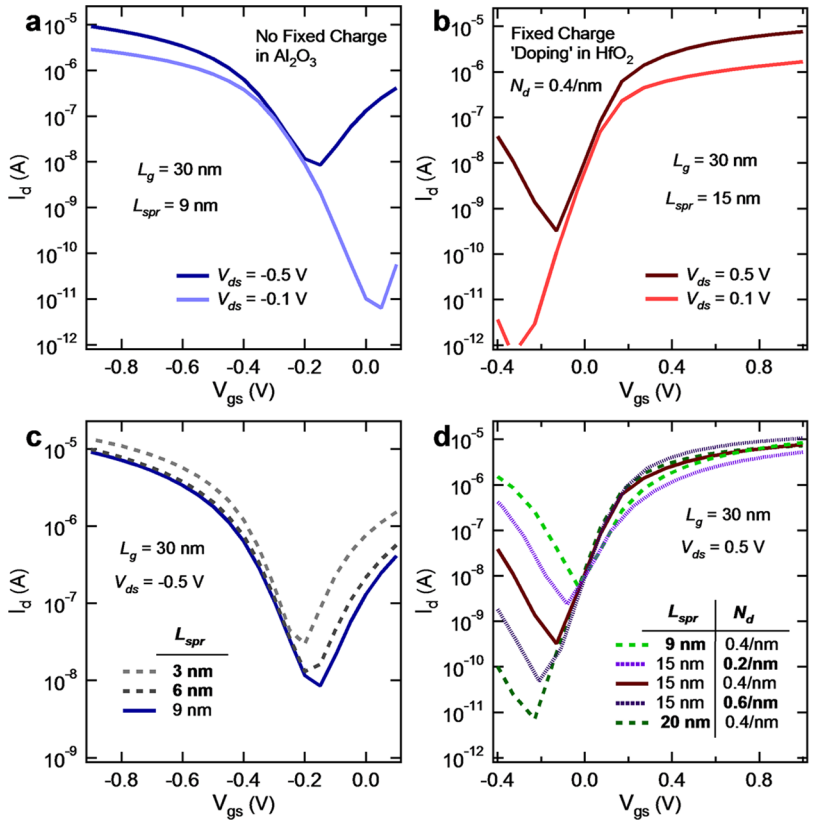

Figure 5. Simulation of p- and n-type GAA-CNTFETs. (a) Subthreshold curves for a 30 nm p-FET with $L_{spr} = t_{ox} = 9$ nm of Al_2O_3. (b) Subthreshold curves for a 30 nm n-FET ($L_{spr} = 15$ nm, $t_{ox} = 9$ nm) obtained by applying a doping density ($N_d = 0.4$/nm) along the CNT to represent the impact of the effectual doping from the AlO_xN_y/HfO_2 dielectric stack. The experimental device in Figure 2e shows good agreement to this simulated device with only a slightly higher SS (99 mV/dec for the experimental device versus 73 mV/dec in the simulation). (c) Impact of spacer length on p-FET performance ($L_{spr} = t_{ox}$), showing how a shorter spacer can boost the on-current at the cost of correspondingly higher off-current. (d) Impact of spacer length and doping density on performance ($t_{ox} = 9$ nm), predominantly affecting the leakage current.

how the spacer length predominantly impacts leakage current for n-FETs and on-current for p-FETs (Figure S8, Supporting Information). Overall, the n-FET exhibits a stronger sensitivity to L_{spr} modulation than the undoped p-FET. Performance for both n- and p-FETs could be further improved if the appropriate doping of the CNT were isolated to the spacer regions, leaving the channel intrinsic, which would boost the on-current, decrease the off-current, and deliver a SS very near the theoretical limit of 60 mV/dec.

While the GAA geometry is ideal for the electrostatic control of a channel at very short lengths, it is important to note that this is largely a negligible motivation for CNTFETs. Recent work has shown that CNTs can yield excellent devices with ultrashort channel lengths using only a bottom gate (cylinder-on-plate)[9] or a top-gate geometry.[35] Hence, while the GAA does yield the best electrostatics, the benefit is minor for CNTs. However, at the high densities envisioned for advanced integration, electrostatic coupling to neighboring nanotubes in the same transistor channel does becomes an issue.[36] Also impactful is the presence of any stray charge (e.g., traps, adsorbates) in the vicinity of the CNT that cause variation in performance.[16] For these challenges—coupling to neighboring CNTs and stray charge effects—the GAA provides the needed isolation of each nanotube. In the specific approach used in this work, the nanotube channels are suspended prior to the dielectric deposition, enabling a complete isolation from any substrate effects followed by encapsulation to avoid any performance degradation. The presence of variation in these devices is now entirely attributed to the quality of the gate dielectric, which has been used as deposited. Annealing and other treatments should enable reduction in interface traps and other quality issues so that the benefits of the GAA are fully realized.

In conclusion, CNTFETs with gates that completely wrap the nanotube channels have been demonstrated. Evidence of the uniformity in GAA coverage was given using TEM cross-sectional imaging. A self-aligned gate contact was established, with devices scaled down to gate lengths of 20 nm. Complementary n- and p- type devices were realized by using HfO_2 and Al_2O_3 gate dielectrics, respectively. Simulations of the GAA-CNTFETs revealed the significance of the spacer regions in determining performance. These results indicate that arrays of nanotubes can be integrated into scalable, self-aligned n- and p-type logic devices with the most ideal gating geometry. Going forward, this accessible approach will enable further studies on GAA-CNTFETs wherein optimization of the gate dielectric and spacer regions will yield further improvements in device performance and consistency.

■ ASSOCIATED CONTENT

Supporting Information

Detailed information on the transistor fabrication process, characterization of the CNTs and devices, details of the gate contact self-alignment, impact of the spacers, capacitance data from the dielectric layers, and details on the numerical simulation with band diagrams for the n- and p-FETs. This

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material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Dennard, R.; Gaensslen, F.; Yu, H.; Rideout, V.; Bassous, E.; LeBlanc, A. *IEEE J. Solid-State Circuits* **1974**, *9*, 256.
(2) Danowitz, A.; Kelley, K.; Mao, J.; Stevenson, J. P.; Horowitz, M. CPU DB: Recording Microprocessor History. http://queue.acm.org/detail.cfm?id=2181798, 2012.
(3) Intel 22 nm 3-D Tri-Gate Transistor Technology. http://newsroom.intel.com/docs/DOC-2032, 2011.
(4) Chang, L.; Frank, D. J.; Montoye, R. K.; Koester, S. J.; Ji, B. L.; Coteus, P. W.; Dennard, R. H.; Haensch, W. *Proc. IEEE* **2010**, *98*, 215−236.
(5) Bernstein, K.; Cavin, R. K.; Porod, W.; Seabaugh, A.; Welser, J. *Proc. IEEE* **2010**, *98*, 2169−2184.
(6) Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. *Nature* **2003**, *424*, 654−657.
(7) Chen, Z.; Appenzeller, J.; Lin, Y. M.; Sippel-Oakley, J.; Rinzler, A. G.; Tang, J.; Wind, S. J.; Solomon, P. M.; Avouris, P. *Science* **2006**, *311*, 1735.
(8) Ding, L.; Liang, S.; Pei, T.; Zhang, Z.; Wang, S.; Zhou, W.; Liu, J.; Peng, L.-M. *Appl. Phys. Lett.* **2012**, *100*, 263116.
(9) Franklin, A.; Luisier, M.; Han, S.-J.; Tulevski, G.; Breslin, C.; Gignac, L.; Lundstrom, M.; Haensch, W. *Nano Lett.* **2012**, *12*, 758−762.
(10) Auth, C. P.; Plummer, J. D. *IEEE Electron Device Lett.* **1997**, *18*, 74−76.
(11) Franklin, A. D.; Sayer, R. A.; Sands, T. D.; Fisher, T. S.; Janes, D. B. *J. Vac. Sci. Technol. B* **2009**, *27*, 821−826.
(12) Chen, Z. H.; Farmer, D.; Xu, S.; Gordon, R.; Avouris, P.; Appenzeller, J. *IEEE Electron Device Lett.* **2008**, *29*, 183−185.
(13) Léonard, F.; Stewart, D. A. *Nanotechnology* **2006**, *17*, 4699−4705.
(14) Guo, J.; Datta, S.; Lundstrom, M. *IEEE Trans. Electron Devices* **2004**, *51*, 172−177.
(15) Koswatta, S. O.; Hasan, S.; Lundstrom, M. S.; Anantram, M. P.; Nikonov, D. E. *IEEE Trans. Electron Devices* **2007**, *54*, 2339−2351.
(16) Franklin, A.; Tulevski, G.; Han, S.; Shahrjerdi, D.; Cao, Q.; Chen, H.-Y.; Wong, H.-S. P.; Haensch, W. *ACS Nano* **2012**, *6*, 1109−1115.
(17) Lin, Y.-M.; Tsang, J. C.; Freitag, M.; Avouris, P. *Nanotechnology* **2007**, *18*, 295202.
(18) Ding, L.; Wang, S.; Zhang, Z.; Zeng, Q.; Wang, Z.; Pei, T.; Yang, L.; Liang, X.; Shen, J.; Chen, Q.; Cui, R.; Li, Y.; Peng, L.-M. *Nano Lett.* **2009**, *9*, 4209−14.
(19) Ding, L.; Zhang, Z.; Liang, S.; Pei, T.; Wang, S.; Li, Y.; Zhou, W.; Liu, J.; Peng, L.-M. *Nat. Commun.* **2012**, *3*, 677.
(20) Javey, A.; Tu, R.; Farmer, D. B.; Guo, J.; Gordon, R. G.; Dai, H. *Nano Lett.* **2005**, *5*, 345−348.
(21) Chen, J.; Klinke, C.; Afzali, A.; Avouris, P. *Appl. Phys. Lett.* **2005**, *86*, 123108.
(22) Klinke, C.; Chen, J.; Afzali, A.; Avouris, P. *Nano Lett.* **2005**, *5*, 555−8.
(23) Ding, L.; Wang, Z.; Pei, T.; Zhang, Z.; Wang, S.; Xu, H.; Peng, F.; Li, Y.; Peng, L.-M. *ACS Nano* **2011**, *5*, 2512−2519.
(24) Zhang, Z.; Wang, S.; Ding, L.; Liang, X.; Pei, T.; Shen, J.; Xu, H.; Chen, Q.; Cui, R.; Li, Y.; Peng, L.-M. *Nano Lett.* **2008**, *8*, 3696−701.
(25) Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. *Nano Lett.* **2004**, *4*, 1319−1322.
(26) Kovacs, G. T. A.; Maluf, N. I.; Petersen, K. E. *Proc. IEEE* **1998**, *86*, 1536−1551.
(27) Farmer, D. B.; Gordon, R. G. *Nano Lett.* **2006**, *6*, 699−703.
(28) Lin, Y.-M.; Jenkins, K. A.; Valdes-Garcia, A.; Small, J. P.; Farmer, D. B.; Avouris, P. *Nano Lett.* **2009**, *9*, 422−6.
(29) Kim, S.; Kim, S.; Janes, D. B.; Mohammadi, S.; Back, J.; Shim, M. *Nanotechnology* **2010**, *21*, 385203.
(30) Guha, S. Results under preparation for publication, 2013.
(31) Zhang, J.; Wang, C.; Fu, Y.; Che, Y.; Zhou, C. *ACS Nano* **2011**, *5*, 3284−3292.
(32) Moriyama, N.; Ohno, Y.; Kitamura, T.; Kishimoto, S.; Mizutani, T. *Nanotechnology* **2010**, *21*, 165201.
(33) Franklin, A. D.; Chen, Z. *Nat. Nanotechnol.* **2010**, *5*, 858−862.
(34) Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Yenilmez, E.; Gordon, R. G.; Lundstrom, M.; Dai, H. *Nano Lett.* **2004**, *4*, 1319−1322.
(35) Choi, S.-J.; Bennett, P.; Takei, K.; Wang, C.; Lo, C. C.; Javey, A.; Bokor, J. *ACS Nano* **2013**, *7*, 798−803.
(36) Raychowdhury, A.; De, V. K.; Kurtin, J.; Borkar, S. Y.; Roy, K.; Keshavarzi, A. *IEEE Trans. Electron Devices* **2009**, *56*, 383−392.