Double Contacts for Improved Performance of Graphene Transistors

Aaron D. Franklin, *Member, IEEE*, Shu-Jen Han, *Member, IEEE*, Ageeth A. Bol, and Vasili Perebeinos

***Abstract*—A new double-contact geometry for graphene devices is studied and compared to traditional top contacts. Double contacts consist of metal below and above the graphene in a sandwich-type configuration. Four-probe structures were tested for both single-layer [chemical-vapor-deposition (CVD)-grown] graphene and bilayer (mechanically exfoliated) graphene, with both showing a decrease in contact resistance of at least 40% and an increase in transconductance greater than 20%. CVD-grown single-layer graphene transistors exhibited contact resistance as low as 260 $\Omega \cdot \mu$m, with an average of 320 $\Omega \cdot \mu$m. This new geometry can help minimize the impact of contacts on graphene device performance.**

***Index Terms*—Contact geometry, contact resistance, double contacts, field-effect transistor, graphene.**

I. Introduction

OWING to reports of graphene's extremely high intrinsic mobility and unique electronic structure [1], [2], along with demonstrations of device cutoff frequencies in the hundreds-of-gigahertz range [3], [4], graphene transistors have become of great interest for electronic applications. As the performance of graphene devices has continued to increase, so also has the understanding of transport properties and performance limitations [5]. It has become apparent that controlling the metal–graphene contact interface is one of the foremost challenges to maximizing performance [6]–[14]. A variety of factors—such as metal-induced doping of the graphene [6], [11]—result in contact resistances that can often dominate the operation of graphene transistors. In this letter, we examine a new double-contact geometry for graphene transistors and assess its value by comparing to traditional top-contacted devices. The result is a substantial improvement in key performance metrics, including contact resistance and transconductance.

II. Device Fabrication

All graphene transistors in this study were four-probe structures, as shown in Fig. 1(e). To establish double contacts, which consist of metal below and above the graphene in the source/drain contact area, bottom contacts were first formed in the substrate [see Fig. 1(a)]. On p^+ Si wafers with 90-nm SiO_2, trenches were fashioned by patterning poly(methyl methacrylate) (PMMA) using e-beam lithography, followed by reactive-ion etching (RIE) the SiO_2 in CF_4 to a depth of 20 nm. The PMMA was then undercut by $\sim$10 nm with a 10-s dip in 9 : 1 buffered oxide etch, followed by the e-beam evaporation and lift-off of 5-nm Ti/25-nm Pd. The Pd surface of the resulting bottom contacts is nominally flush with the SiO_2 to support the graphene on a level surface [see Fig. 1(d)].

Two types of graphene were studied: 1) single-layer graphene that was grown by chemical vapor deposition (CVD) on Cu foils and then transferred [15], [16] to the substrate containing bottom contacts and 2) bilayer graphene that was mechanically exfoliated from graphite flakes [1]. The advantage for CVD-grown films is the large coverage area; in this study, an entire 2 cm $\times$ 2 cm chip was covered with the single-layer graphene. Such coverage enabled the fabrication of a large set of devices, providing a statistical distribution that could not be similarly obtained using mechanical exfoliation. Following transfer and O_2 RIE patterning of the graphene, top contacts were formed (0.5-nm Ti/30-nm Pd/30-nm Au) with a maximum offset of 20 nm from bottom contacts in double-contact configuration. The devices were annealed in vacuum at 130 °C for 10 h prior to being electrically tested.

III. Results and Discussion

The transfer characteristics comparing double-, bottom-, and top-contacted devices are shown in Fig. 2. Improvement in current is seen for both types of graphene in the double-contact geometry but is more pronounced in the bilayer case. In both cases, the enhancement in current is greater at high gate bias (far away from the Dirac point); this is evidence of a decrease in contact resistance, which dominates at gate biases that are far from the neutrality point.

A more thorough analysis is obtained using the additional voltage probes (V_1 and V_2) shown in Fig. 1(e). Importantly, these voltage probes are external from (or noninvasive to) the graphene channel, keeping them from perturbing transport in the channel by induced doping [6], [9], [11]. The most useful aspect of the four-probe structure is a clean extraction of the contact resistance (R_c) as follows:

$$R_c = \frac{1}{2}\left(R_{2p} - R_{4p}\frac{L_{2p}}{L_{4p}}\right)W$$

where R_{2p} is the resistance between the source and drain contacts, R_{4p} is the resistance between the voltage probes (V_1

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The authors are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA (e-mail: aaronf@us.ibm.com; sjhan@us.ibm.com; ageethbol@gmail.com; vperebe@us.ibm.com).

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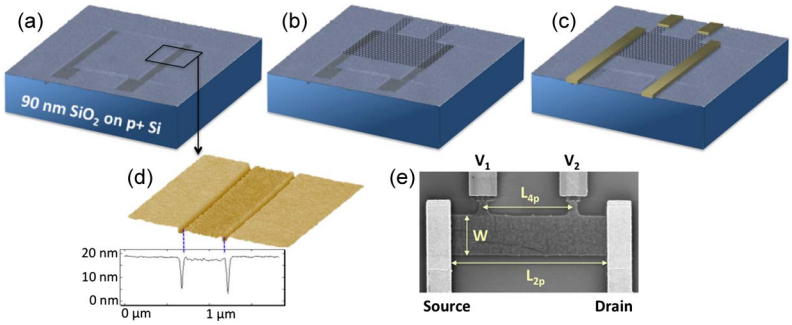

Fig. 1. (a) Tilted false-colored atomic force microscope (AFM) surface plot of Pd bottom contacts embedded in 90-nm SiO_2. (b) Graphene transferred onto bottom contacts and then patterned/etched into a four-probe structure. (c) Top contacts (Pd) established with the source/drain aligned directly onto bottom contacts, forming a double-contact geometry. (d) Higher magnification AFM image showing the bottom contact surface within < 1 nm of surrounding SiO_2. (e) Scanning electron microscope (SEM) image of a completed four-probe device with relevant dimensions and contacts identified. For all devices in this work, $W = 1$ μm, $L_{2p} = 3.5$ μm, and $L_{4p} = 2$ μm. Note that the p^+ Si substrate is used as the gate for transistor operation (V_{gs}).

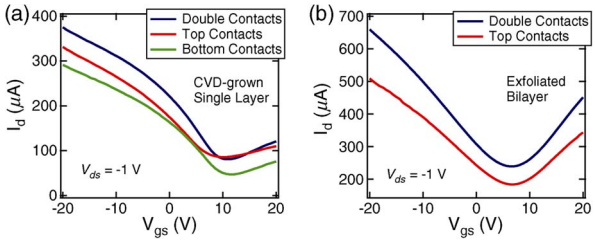

Fig. 2. Transfer characteristics from top-, bottom-, and double-contacted graphene transistors fabricated with (a) CVD-grown single-layer graphene and (b) mechanically exfoliated bilayer graphene.

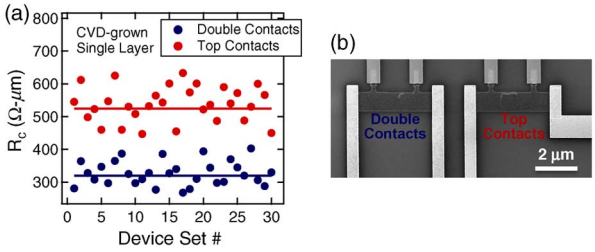

Fig. 3. (a) Contact resistance distribution from all single-layer graphene devices tested; R_c was taken at $V_{\rm gs} - V_{\rm Dirac} = -20$ V. In spite of significant variation, the devices with double contacts consistently exhibited lower R_c than those with only top contacts. The lowest R_c's for each geometry are 450 $\Omega \cdot \mu$m for the top contacts and 260 $\Omega \cdot \mu$m for the double contacts. The horizontal lines indicate the average value. (b) SEM image of a device set, with the double-contacted device on the left and the top-contacted device on the right.

and V_2), and L_{2p}, L_{4p}, and W are the dimensions defined in Fig. 1(e).

When working with graphene (particularly CVD grown), there can be a considerable amount of variation in the cleanliness and/or quality of the graphene surface after undergoing transfer. This is another reason why the four-probe structure is vital in that it considers the resistance of each device's graphene channel to extract the resistance at its contacts, thus allowing for a fair comparison of R_c for different devices. In this study, 30 sets of single-layer devices were tested, with each set having side-by-side graphene transistors—one with double contacts and one with top contacts for the source and drain—as shown in Fig. 3(b). Also studied was a set of 12 bottom-contacted devices that were also on single-layer graphene. All voltage probes (V_1 and V_2) were top contacts because the resistance of these contacts does not affect their sole purpose of monitoring voltage.

TABLE I
AVERAGED VALUES OF KEY METRICS FROM ALL DEVICE SETS OF TOP-, BOTTOM-, AND DOUBLE-CONTACTED GRAPHENE TRANSISTORS

Graphene / Layers	Contact	R_c (Ω-µm)[a]	g_m (µS)	μ_{peak} (cm^2/Vs)
CVD / Single	Double	320	21	1910
CVD / Single	Top	525	16	1460
CVD / Single	Bottom	715	18	1540
Exfoliated / Bilayer	Double	250	35	3190
Exfoliated / Bilayer	Top	580	29	2640

[a] R_c was taken at $V_{gs} - V_{dirac} = -20$ V.

The distribution of contact resistance for the double- and top-contacted single-layer graphene device sets is shown in Fig. 3(a). It can be seen why having a large sample set is essential for drawing conclusions about the quality of a certain contact geometry. Just as the quality of the graphene channel can vary across a chip, so also can the condition of the graphene that interfaces with the contact metal (local defects, residual resist, etc.). Therefore, a sizeable amount of variation in R_c is observed, even when fabricating transistors with the same geometry and in very close proximity on a chip. Despite this variation, the plot in Fig. 3 reveals that the double-contacted graphene transistors consistently exhibited lower R_c than their top-contacted counterparts.

A summary of some key performance metrics comparing the double-, bottom-, and top-contacted devices is given in Table I. While there were 30 (12) sets of devices for the double- and top-contacted (bottom-contacted) single-layer graphene that contributed to these averaged values, the exfoliated bilayer devices were much harder to come by because they relied on random placement of the graphene onto predefined bottom contacts; however, the data for the bilayer devices are an average from 6 sets. There is a nearly 40% drop in R_c going from top- to double-contacted single-layer devices, which averaged 320 $\Omega \cdot \mu$m with a low of 260 $\Omega \cdot \mu$m, which is—to our knowledge—the lowest reported contact resistance for a CVD-grown single graphene layer, with previous reports (from various graphene sources) falling in the 500- to 1000-$\Omega \cdot \mu$m range [7], [12], [17]. The bilayer double-contacted devices reached an even lower average R_c of 250 $\Omega \cdot \mu$m, with a low of 180 $\Omega \cdot \mu$m. As for the improvement in average peak transconductance g_m (and, correspondingly, the peak field-effect mobility $\mu_{\rm peak}$), they were 31% and 21% in the single and bilayer cases, respectively.

The reason for g_m and $\mu_{\rm peak}$ improving less than R_c is that improvement of the contacts is more clearly observed when the graphene is biased far from the Dirac point (in the ON state). It is when $V_{\rm gs}$ is swept closer to the Dirac point that the resistance in the graphene channel dominates and more dramatic modulation of the current takes place to yield the peak g_m (thus $\mu_{\rm peak}$) value, as seen in the characteristics in Fig. 2. Take, for instance, the higher average mobility observed in the bottom-contacted devices compared to the top-contacted ones, even though the contact resistance is higher.

While the bottom-contacted devices are not on the same graphene channels as the double-contacted devices, the average R_c from the different device sets does provide insight into the improved performance. Unlike in the top-contacted device, the substrate gate does not influence the doping level of the graphene in the source/drain areas for the bottom-contacted device. Therefore, the 36% higher contact resistance in bottom-contacted devices can be attributed to the lower doping level. Using an electrostatic model similar to that in [18] with an effective graphene–metal distance $d = 1$ Å and $W_{\rm Pd} - W_G - \Delta_c = 200$ meV, where $W_{\rm Pd}$ and W_G are the palladium and graphene work functions, respectively, and Δ_c is due to the correlations [19], the observed differences in R_c can be better understood. For double-contacted graphene, this model (using $C_g = \varepsilon_0/d$ and $V_{\rm gs} = 0$) predicts a 23% lower doping level than that in the top-contacted device. Taking into account that a factor of two larger graphene–metal coupling translates to a $\sqrt{2}$ reduction in R_c in a diffusive contact [18], we would expect a contact resistance of 460 $\Omega \cdot \mu$m in double-contacted devices. This is 40% larger than the measured resistance of 320 $\Omega \cdot \mu$m. We attribute this remaining difference to a higher metal-induced doping in double-contacted graphene than in the one-sided geometries owing to the increased coverage of metal on graphene.

In the bilayer graphene case, the reduction of R_c by approximately a factor of two is expected in electrically decoupled, i.e., misoriented, layers—carrier injection takes place for each layer independently. Analysis of AB stacked bilayer is more complicated due to the uncertainty in the ratio of transfer length and an electrical coupling between the layers, which determines an overall contact resistance reduction in the range of $\sqrt{2}$–2. Ultimately, the double-contacted bilayer graphene creates a carrier transport scenario that warrants its own complete study of transport physics.

IV. Conclusion

In conclusion, we have demonstrated that a double-contact geometry (metal below and above graphene at the source and drain) provides improved graphene transistor performance compared to traditional top contacts. Dozens of double- and top-contacted four-probe structures were tested to show a consistent reduction of contact resistance and improvement of transconductance. On average, R_c dropped from 525 to 320 $\Omega \cdot \mu$m for single-layer graphene. We attribute the observed improvement in contact resistance to both an enhancement of the effective graphene–metal coupling and a higher graphene doping in the presence of the second metal layer.

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