Effects of Nanoscale Contacts to Graphene

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Abstract—Understanding and optimizing transport between metal contacts and graphene is one of the foremost challenges for graphene devices. In this letter, we present the first results on the effects of reducing contact dimensions to the nanoscale in single-layer graphene transistors. Using noninvasive voltage probes to the graphene channel, the contact resistance was extracted and observed to increase dramatically at contact lengths below 200 nm. Also affected was the extrinsic transconductance, reducing by more than 70% when scaling the contacts from 200 to 50 nm. No significant change in performance per unit width was observed when reducing the contact/device width from 500 to 80 nm. These results provide key insights into the ultimate scalability of graphene transistors, particularly when considering them for a densely integrated technology.

Index Terms—Contact resistance, field-effect transistor, graphene, length scaling.

I. INTRODUCTION

▼ RAPHENE is a single atomic sheet of carbon atoms in \mathbf{J} an sp^2 -bonded honeycomb lattice. In spite of being a simple monolayer, intrinsic graphene can carry impressively high current densities at mobilities nearing $200\,000 \text{ cm}^2/\text{V} \cdot \text{s}$ [1]. These, and other unique electrical properties, have enabled graphene transistors to deliver cutoff frequencies in the range of hundreds of gigahertz [2], [3]. When considering the other advantages that graphene offers, such as transparency and flexibility [4], [5], it is clear why this material is of such great interest for a myriad of electronic applications. Depending on the application, there could be a need for achieving a high packing density of graphene transistors by scaling down channel and contact dimensions. While there have been some recent works on the impact of channel length scaling [6], there is very limited information on the impact of reducing the size of the contacts.

In this letter, the impact of shrinking metal–graphene contacts to nanoscale dimensions is presented. More than 100 single-layer graphene transistors were tested with contact lengths (L_c) ranging from 500 to 20 nm having constant widths (W) of 1 μ m. Another set of devices had a variation in width from 500 to 80 nm and a constant contact length of 500 nm. All transistors were in a four-probe configuration, which enabled straightforward extraction of the contact resistance (R_c) .

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A trend was observed showing a strong dependence of R_c on contact length when $L_c < 200$ nm and no observable dependence on width.

II. DEVICE FABRICATION

The devices in this study were fabricated from single-layer graphene grown using chemical vapor deposition (CVD) on copper foils [9]. Graphene was transferred from the foil to a p^+ doped silicon substrate with 90-nm thermal SiO₂. Electronbeam lithography using a polymethyl methacrylate (PMMA) resist was used to define the shape of the graphene devices by employing an oxygen plasma reactive-ion etch to remove the exposed regions of graphene. Next, source/drain contacts were lithographically defined, followed by deposition of 0.5-nm Ti/20-nm Pd/30-nm Au and subsequent lift-off of PMMA in hot acetone. All electrical testing was performed in vacuum (10^{-7} torr) and at room temperature after a 10-h vacuum anneal of the devices at 120 °C.

The layout of the four-probe-configuration device structure is shown in Fig. 1(a). All L_c -scaled devices had a width Wof 1 μ m, while L_c (which is the same for source and drain in a given device) was varied. The dimensions of the voltage probes V_1 and V_2 were kept constant. The scanning electron microscope (SEM) images of the representative devices with four different contact lengths are shown in Fig. 1(b). As can be seen in these SEM images, defects such as domain boundaries or wrinkles occur randomly from device to device, necessitating the testing of a large set of devices to ensure an accurate statistical distribution. The substantial advantage that CVDgrown graphene offers is the complete coverage of a substrate, allowing for the fabrication of many devices [10]—this affords enough data to minimize the impact of variation in graphene film quality.

III. RESULTS AND DISCUSSION

To determine the graphene film quality and confirm that it is a single layer, Raman spectroscopy was performed, and the resulting spectrum is shown in Fig. 2(b). The presence of a sharp and intense 2-D peak denotes that graphene is a monolayer, while the substantial G/D ratio indicates that the quality is high, particularly for CVD-grown graphene. Grain size was measured in similar graphene films (grown using the same process) using low-energy electron microscopy and is approximately 10 μ m—much larger than the device structures in this study.

The transfer characteristics from a representative set of graphene transistors are shown in Fig. 2(a). These characteristics were obtained using the doped silicon substrate as a back gate $(V_{\rm gs})$ and the source/drain contacts in a standard



Fig. 1. (a) Schematic of the four-probe device structure with relevant dimensions specified. The substrate is 90-nm SiO₂ on p⁺ doped Si. For the L_c -scaled devices in this work, $W = 1 \mu m$, $L_{2p} = 3.5 \mu m$, and $L_{4p} = 2 \mu m$, while L_c is varied. Note that the p⁺ Si substrate is used as the gate for transistor operation (V_{gs}). (b) SEM images of four graphene devices with different contact lengths. These devices are from CVD-grown single-layer graphene.



Fig. 2. (a) Transfer characteristics from transistors of CVD-grown single-layer graphene with an L_{2p} (channel length) of 3.5 μ m and a width of 1 μ m, over a range of L_c (contact length) from 200 to 20 nm. (b) Raman spectra at a 532-nm excitation wavelength, confirming single-layer (sharp 2-D peak) and high-quality (high G/D ratio) graphene.



Fig. 3. (a) Contact resistance and peak extrinsic transconductance dependence on contact length. The data points denote the average values with error bars indicating the high and low points. The noted $V_{\rm gs}$ corresponds to the point of R_c extraction. (b) Contact resistance dependence on width. The width is the same for both the channel and the graphene beneath the source/drain contacts. The dashed line indicates the average of all data points from every width.

field-effect transistor structure. Note the distinct decline in performance as L_c is scaled down, specifically with respect to current and on/off ratio.

The contact resistance for each device can be extracted using the two voltage probes. Importantly, these voltage probes are external from (or noninvasive to) the graphene channel, keeping them from perturbing transport in the channel by induced doping [11]–[13]. Extracting contact resistance using the fourprobe structure can be done as follows:

$$R_c = \frac{1}{2} \left(R_{2p} - R_{4p} \frac{L_{2p}}{L_{4p}} \right) W$$

where R_{2p} is the resistance between the source and drain contacts, R_{4p} is the resistance between the voltage probes (V_1 and V_2), and L_{2p} , L_{4p} , and W are the dimensions defined in Fig. 1(a).

A plot of the contact resistance versus contact length is shown in Fig. 3(a), along with the peak extrinsic transconductance (g_m) , which includes the influence of the contacts. At contact lengths above 200 nm, there is very little variation in R_c (or g_m); this indicates that L_c has become much greater than the transfer length (L_T) . The transfer length is the length over which the potential drops to 1/e of the applied V_{ds} [14] and generally denotes the length of the contact wherein carrier injection is taking place (in this case, between metal and graphene). The steep drop in transconductance associated with increasing R_c is a result of the contact resistance beginning to dominate the device.

Recently, results have been reported for contact length scaling in carbon nanotube (CNT) transistors [15]. The interface between a metal and a CNT is similar to that between metal and graphene because a nanotube is structurally a rolled sheet of graphene, made from the same sp^2 -bonded carbon.

Importantly, both materials exhibit R_c dependence on L_c below approximately 200 nm, contrary to the oft-proposed picture of purely edge conduction without length dependence [16]. Note that this similarity in R_c-L_c behavior is despite the CNT in [15] being a semiconductor, while graphene is more like a semimetal (zero bandgap).

Another point concerning the contact length scaling data is regarding the general contact resistivity (ρ_c). A recent report [16] suggested that transport between a metal contact and graphene may be edge dominated based on a plot of ρ_c versus contact area. The idea is that resistivity should be a constant regardless of the dimensions of the device (ignoring other local variations), and thus, a plot of $\rho_c = R_c A$ (where A is the contact area, $L_c \times W$) and $\rho_c = R_c W$ may reveal whether the contact length is an important dimension. Data from the report showed that $\rho_c = R_c W$ gives a more constant resistivity than the area-dependent case, leading the authors to suggest that transport happens entirely at the contact edge. However, the reason for this observation is that $L_c \gg L_T$ for the devices studied in the report, giving the impression of edge conduction. The devices in this study have contact lengths that fall well below and above the transfer length, providing a more accurate picture in the plot in Fig. 3(a).

Because of the unique 3-D-metal-to-2-D-graphene interface, other dimensions could play a role in determining the R_c-L_c curve. A recent report [17] showed that R_c for graphene devices is determined by the following two key components: 1) the injection of carriers from the metal to graphene and 2) the transport of the carriers from metal-covered graphene to the graphene channel. Therefore, the width of the contacts to graphene could alter the dependence of resistance on the contact length.

To test the possible dependence of R_c on W, devices were studied with widths from 500 down to 80 nm, having a constant L_c of 500 nm. Fig. 3(b) shows that there is no noticeable dependence of R_c on the width (which is the same both in the channel and under the contacts). While the smaller width devices do show a larger distribution in R_c , the average from each set of 12 or more devices is very consistent across all widths studied. One reason for the larger R_c distribution for small-W devices is that a defect in the graphene channel will cause substantial impact on an 80-nm-wide device but only minimal impact on a 500-nm device. Another contributing factor could be the opening of a small bandgap in the W-scaled devices [18]. Overall, this evidence of no width dependence for R_c is significant when considering the scalability of contacts to graphene devices.

IV. CONCLUSION

In conclusion, a strong dependence of contact resistance on nanoscale contact length has been observed from a large set of single-layer CVD-grown graphene transistors having L_c from 500 down to 20 nm. All devices were in a fourprobe configuration, enabling straightforward extraction of the contact resistance. Above 200 nm, contact length has minimal impact on R_c , which is indicative of L_c being longer than the transfer length. Additionally, the device width was scaled from 500 to 80 nm without significant change in contact resistance.

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REFERENCES

- X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene," *Nat. Nanotechnol.*, vol. 3, no. 8, pp. 491–495, Aug. 2008.
- [2] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a selfaligned nanowire gate," *Nature*, vol. 467, no. 7313, pp. 305–308, Sep. 2010.
- [3] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and Ph. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, Feb. 2010.
- [4] A. Kasry, M. A. Kuroda, G. J. Martyna, G. S. Tulevski, and A. A. Bol, "Chemical doping of large-area stacked graphene films for use as transparent, conducting electrodes," *ACS Nano*, vol. 4, no. 7, pp. 3839–3844, Jul. 2010.
- [5] B. J. Kim, H. Jang, S.-K. Lee, B. H. Hong, J.-H. Ahn, and J. H. Cho, "High-performance flexible graphene field effect transistors with ion gel gate dielectrics," *Nano Lett.*, vol. 10, no. 9, pp. 3464–3466, Sep. 2010.
- [6] L. Liao, J. Bai, R. Cheng, Y.-C. Lin, S. Jiang, Y. Qu, Y. Huang, and X. Duan, "Sub-100 nm channel length graphene transistors," *Nano Lett.*, vol. 10, no. 10, pp. 3952–3956, Oct. 2010.
- [7] Q. Zhang, Y. Lu, H. G. Xing, S. J. Koester, and S. O. Koswatta, "Scalability of atomic-thin-body (ATB) transistors based on graphene nanoribbons," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 531–533, Jun. 2010.
- [8] S.-J. Han, Y. Sun, A. A. Bol, W. Haensch, and Z. Chen, "Study of channel length scaling in large-scale graphene FETs," in *VLSI Symp. Tech. Dig.*, 2010, pp. 231–232.
- [9] X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Largearea synthesis of high-quality and uniform graphene films on copper foils," *Science*, vol. 324, no. 5932, pp. 1312–1314, Jun. 2009.
- [10] H. Yamaguchi, G. Eda, C. Mattevi, H. Kim, and M. Chhowalla, "Highly uniform 300 mm wafer-scale deposition of single and multilayered chemically derived graphene thin films," ACS Nano, vol. 4, no. 1, pp. 524–528, Jan. 2010.
- [11] P. Blake, R. Yang, S. V. Morozov, F. Schedin, L. A. Ponomarenko, A. A. Zhukov, R. R. Nair, I. V. Grigorieva, K. S. Novoselov, and A. K. Geim, "Influence of metal contacts and charge inhomogeneity on transport properties of graphene near the neutrality point," *Solid State Comm.*, vol. 149, no. 27/28, pp. 1068–1071, Jul. 2009.
- [12] S. Barraza-Lopez, M. Vanevic, M. Kindermann, and M. Y. Chou, "Effects of metallic contacts on electron transport through graphene," *Phys. Rev. Lett.*, vol. 104, no. 7, p. 076 807, Feb. 2010.
- [13] B. Huard, N. Stander, J. A. Sulpizio, and D. Goldhaber-Gordon, "Evidence of the role of contacts on the observed electron-hole asymmetry in graphene," *Phys. Rev. B*, vol. 78, no. 12, pp. 121402-1–121402-4, Sep. 2008.
- [14] D. K. Schroder, Semiconductor Material and Device Characterization. Hoboken, NJ: Wiley, 2006.
- [15] A. D. Franklin and Z. Chen, "Length scaling of carbon nanotube transistors," *Nat. Nanotechnol.*, vol. 5, no. 12, pp. 858–862, Dec. 2010.
- [16] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Appl. Phys. Lett.*, vol. 97, no. 14, pp. 143 514-1–143 514-3, Oct. 2010.
- [17] F. Xia, V. Perebeinos, Y.-M. Lin, Y. Wu, and Ph. Avouris, "The origins and limits of metal–graphene junction resistance," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 179–184, Mar. 2011.
- [18] M. Y. Han, B. Ozyilmaz, Y. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," *Phys. Rev. Lett.*, vol. 98, no. 20, p. 206 805, May 2007.