Current Scaling in Aligned Carbon Nanotube Array Transistors With Local Bottom Gating

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***Abstract*—A local-bottom-gate (LBG) configuration is introduced for carbon nanotube array field-effect transistors (FETs) (CNTFETs). CNTFETs from highly aligned nanotubes are demonstrated and exhibit the best performance to date, with current density $> 40\ \mu A/\mu m$ (with no metallic nanotubes), inverse subthreshold slope of 70 mV/decade, and ON/OFF-current ratio $> 10^5$. Additionally, ON-current from LBG-CNTFETs is shown to scale linearly with the number of nanotube channels. These advancements in device geometry and performance provide a new platform for further progress to be made toward high-performance FETs from aligned nanotubes.**

***Index Terms*—Carbon nanotube (CNT), field-effect transistor (FET), length scaling, local gate, multichannel array.**

I. Introduction

CARBON nanotube array field-effect transistors (CNTFETs) remain one of the most promising options for a next-generation transistor switch with, among other attributes, ballistic transport and an excellent 1-D electronic structure [1]. The integration of CNTFETs must be accomplished using multiple single-walled CNTs (SWCNTs) in each transistor to boost the ON-current high enough for driving chip-level functionality [2]. Significant progress has been made in growing aligned SWCNTs on quartz substrates [3]–[5], followed by the transfer of the nanotubes to a different substrate for integration into multinanotube devices [3], [6]. Most devices with aligned SWCNT arrays have involved thin-film transistors (TFTs) where the channels are long and the widths are hundreds of micrometers [4]–[7]. Other devices that are not TFTs still use wide widths with slightly shorter channels ($\sim 0.5-1\ \mu$m) [8].

This letter presents aligned SWCNT arrays integrated for the first time into transistors with scaled channel length ($L_g \approx 100-150$ nm) and contact width ($W \approx 1-2\ \mu$m) using a local bottom gate (LBG) geometry [Fig. 1(d)]. Contributions to the ON-current from metallic and semiconducting SWCNTs (m- and s-CNTs) are analyzed, and importantly, the ON-current for the CNTFETs (only s-CNTs) is observed to scale directly with the number of nanotube channels. Device results confirm that the LBG gate structure enables a CNT technology that has the potential to compete with projected Si technology in high-performance applications.

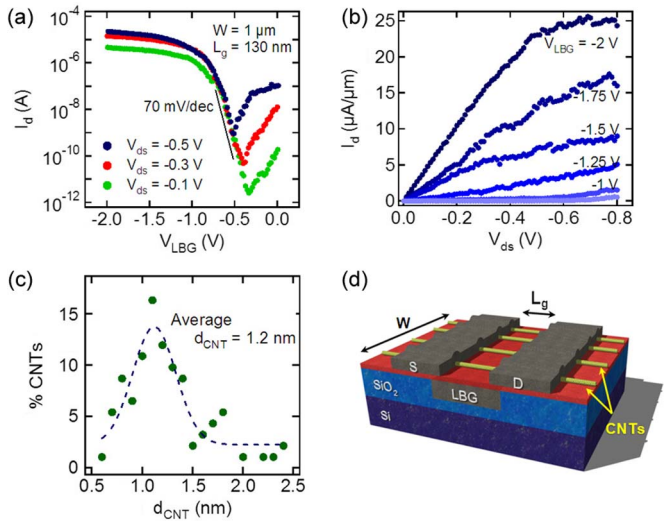

Fig. 1. LBG-CNTFET with aligned nanotubes. Device of $W = 1\ \mu$m with $L_g \approx 130$ nm and 3 SWCNTs/μm (all s-CNTs in this device). (a) Subthreshold curves at different V_{ds}, exhibiting a very low $SS \approx 70$ mV/dec. (b) Output characteristics of the same device, plotted in units of current per contact width, saturating at $\sim 25\ \mu A/\mu m$. (c) Diameter distribution (from atomic force microscope) of the SWCNTs used to fabricate devices in this work. (d) Schematic of the device structure.

II. Device Fabrication

The CNTFETs are fabricated using an LBG geometry. The gate structures are defined by creating trenches in SiO_2 using a combination of dry (reactive ion etch) and wet (buffered oxide etch) etchings (final trench depth ≈ 50 nm). The gate metal is then deposited (10-nm Ti/40-nm Pd), and following lift-off, the Pd gate surface is nominally planar with the surrounding SiO_2. Atomic layer deposition (ALD) is then used to deposit a 10-nm HfO_2 ($\kappa \approx 16-20$)—with equivalent oxide thickness (EOT) of $\sim$2 nm. Aligned SWCNTs, grown on quartz substrates, are then transferred using a technique described elsewhere [3], [6]. Source/drain contacts of 0.5-nm Ti/30-nm Pd/30-nm Au are then formed to complete the LBG-CNTFETs. The final device is shown in Fig. 1(d).

Several advantages are gleaned from the LBG geometry. First, having the gate level with the surrounding SiO_2

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TABLE I
CURRENT-PER-WIDTH COMPARISON

Source[a]	Data	L_g	W	EOT	# SWCNTs	V_{ds}	I_d with m-CNTs	I_d only s-CNTs
Avg. (this work)	Avg	0.13 μm	2 μm	~2 nm	4 /μm	-0.5 V	41 μA/μm	26 μA/μm
High (this work)	Single	0.13 μm	2 μm	~2 nm	5 /μm	-0.5 V	58 μA/μm	42 μA/μm
Ref [5]	Single	12 μm	200 μm	>1 μm	5 /μm	-0.5 V	2.8 μA/μm	1.9 μA/μm
Ref [7]	Single	0.7 μm	100 μm	~20 nm	5 /μm	-0.5 V	50 μA/μm	--
Ref [6]	Single	0.5 μm	100 μm	50 nm	2-3 /μm	-1 V	20 μA/μm	~2 μA/μm
Ref [14]	Single	1 μm	50 μm	50 nm	2 /μm	-1 V	~8 μA/μm	1.4 μA/μm
Ref [15]	Single	1 μm	50 μm	~2 nm	4 /μm	-1 V	--	4.7 μA/μm

[a]Average and single highest values in this work are compared to reported values from various related devices in the literature (all devices involved aligned SWCNTs). "Single" implies extraction from a single device as opposed to an average of many devices, and is from the highest reported data point.

minimizes the bending of the SWCNTs—a key benefit since even minor distortion of SWCNTs can affect their electronic structure and result in carrier transport degradation [9]. Second, the LBGs enable the use of ultrathin dielectrics and, thus, improved electrostatics. A minimum of 8–10 nm is needed to cover SWCNTs in a top-gate geometry [10], but the minimum dielectric thickness for LBG-CNTFETs is determined only by the roughness of the gates. The present devices use a 10-nm HfO_2, for initial demonstration, but this can be scaled further.

III. RESULTS AND DISCUSSION

Characteristics from an LBG-CNTFET are shown in Fig. 1(a) and (b). This device has an L_g of 130 nm and a W of 1 μm with three SWCNTs, all three of which are s-CNTs. Note the relatively small average diameter of the nanotubes ($d_{\mathrm{CNT}} \approx 1.2$ nm) used in this study compared with other chemical-vapor-deposition-grown nanotubes, which tend to be closer to 2 nm [10]. Smaller d_{CNT} nanotubes typically yield higher ON/OFF-current ratios and larger Schottky barrier (SB) heights—both result from the correspondingly larger band gap ($E_g \alpha 1/d_{\mathrm{CNT}}$) [1]. While the high ON/OFF ratios are clearly observed here, the devices remain free of the normally severe degradation caused by SBs. For instance, the inverse subthreshold slope (SS) is usually enlarged by SB tunneling hampering the thermally driven transport; yet, in this case, SS is very near the theoretical limit (60 mV/dec). It is the improved electrostatics of the LBG geometry that provides thinned nearly transparent SBs.

In the past, it has been customary to cite SWCNTs as having current densities on the order of 10^9 A/cm^2, as calculated based solely on the nanotube dimensions ($d_{\mathrm{CNT}} \approx 2$ nm). However, to accurately compare CNTFETs to current Si technology, the entire contact width for the nanotube devices must be accounted for. A comparison of the current per width, along with several other significant parameters from a variety of aligned array CNTFET reports, is given in Table I.

The top row of Table I is for the average data obtained from dozens of LBG-CNTFETs in this work. Because there is a mixture of m- and s-CNTs, the current per width is given for the following: 1) devices that still contain the m-CNTs and 2) devices that have just the s-CNTs. Selective removal of the m-CNTs was accomplished in all cited cases (and in the present work) using electrical breakdown [11]. For the devices

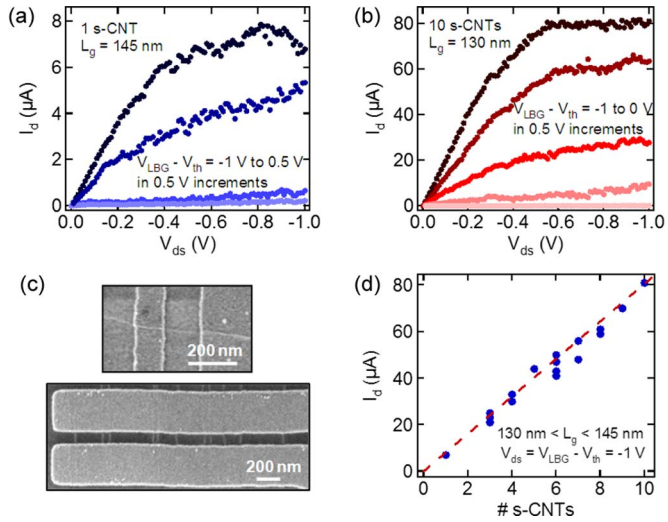

Fig. 2. Demonstration of ON-current scaling directly with the number of s-CNT channels. Output characteristics from LBG-CNTFETs with (a) one s-CNT ($d_{\mathrm{CNT}} \approx 1.2$ nm) and (b) ten s-CNTs over the same range of $V_{\mathrm{LBG}} - V_{\mathrm{th}}$. Gate lengths and contact widths ($W \approx 2$ μm) are nominally the same for both devices. (c) Scanning electron microscope images of the single- and multiple-s-CNT devices (note that some of the SWCNTs for the multichannel device are m-CNTs that were burned out). (d) ON-current versus number of s-CNTs from a set of LBG-CNTFETs at the same overdrive. Note the clear linear scaling of the current with the number of nanotubes.

still containing m-CNTs, the high currents obtained in the present work are a result of the scaled L_g reducing scattering events.

While the current per width with m-CNTs is slightly higher in this work, the current with only s-CNTs is an order of magnitude greater than those of previous studies. Other factors besides L_g scaling are enabling this dramatic current enhancement—improved gate electrostatics and/or a higher percentage of s-CNTs, for instance. Ultimately, these are the first values for current density extracted from scaled CNTFETs of aligned SWCNTs, and they provide a good reference point for what is achievable using a low density (~ 4 SWCNTs/μm) of nanotubes.

When packing many SWCNTs into a device, the predicted ON-current is often hampered by charge screening [12]. Such screening is part of the reason that transistors from solution-deposited SWCNTs (often bundled) exhibit lower than anticipated ON-currents [13]. Therefore, demonstrating the direct scaling of the ON-current with the number of nanotube channels has proven elusive. The modest density of 4 SWCNTs/μm in

this work provides a great platform for observing direct ON-current scaling.

The output characteristics in Fig. 2(a) are from an LBG-CNTFET with a single s-CNT, while those in Fig. 2(b) are from a device with ten s-CNTs (the m-CNTs have been removed). Note the corresponding increase in ON-current between the single- and multinanotube devices as the curves are plotted for the same gate overdrive $(V_{\rm LBG} - V_{\rm th})$. The device in Fig. 2(a) provides the approximate ON-current per s-CNT at these dimensions.

Fig. 2(d) shows a plot of the ON-current versus the number of s-CNTs at the same overdrive $(V_{\rm ds} = V_{\rm LBG} - V_{\rm th} = -1\ {\rm V})$ from different LBG-CNTFETs. The trend is linear, representing direct ON-current scaling. The slight deviation of data points from the linear fit is due to different $d_{\rm CNT}$ nanotubes used in the devices, resulting in varying band gaps and, thus, ON-currents. Further increase in the number of s-CNT channels should allow for greater averaging of the current and, thus, less deviation from the linear fit. Note that, once the spacing between nanotubes becomes $<\sim$5 nm (sum of $d_{\rm CNT}$ and EOT), there will be charge screening to account for in the ON-current scaling [12]. Ideally, work will be done to further increase the density of nanotubes while keeping them unbundled and evenly spaced.

Several years ago, a top-gated CNTFET $(d_{\rm CNT} \approx 1.7\ {\rm nm})$ showed ON-current of $\sim$20 μA at $L_g \approx 50$ nm with EOT $\approx$ 2 nm [10]. For years, this performance was difficult to match, particularly with smaller $d_{\rm CNT}$ nanotubes. Recently, however, using this LBG geometry, a CNTFET $(d_{\rm CNT} \approx 1.2\ {\rm nm})$ exhibited $\sim$18 μA at $L_g \approx 38$ nm and EOT ≈ 2 nm [1]. Such performance using a smaller diameter SWCNT is evidence of improved electrostatics using the LBG geometry. Using these single-nanotube devices as baselines for the achievable current per SWCNT upon further L_g scaling, a device containing 200 s-CNT channels per micrometer (consistent pitch $\sim$5 nm) would provide $\sim$4 mA/μm, which is well beyond the projected Si technology.

IV. Conclusion

A novel LBG geometry was introduced for CNTFETs comprising aligned nanotube arrays, and ON-current was shown to scale linearly with the number of nanotube channels. The LBG geometry improves the CNTFET electrostatics and allows the dielectric to be scaled without a minimum thickness requirement. Furthermore, the LBG-CNTFETs exhibit the highest current density ($>$ 40 μA/μm, without m-CNTs) reported to date with an SS of 70 mV/dec using a modest average of 4 SWCNTs/μm. The next steps toward high-performance aligned CNTFETs should involve increasing nanotube density, further scaling the channel length, and tightening the diameter distribution; all of which are underway.

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