Scalable and Fully Self-Aligned n-Type Carbon Nanotube Transistors with Gate-All-Around

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Abstract

While proven to provide high performance at sub-10 nm lengths, carbon nanotube (CNT) field-effect transistors (FETs) typically employ impractical gate geometries. Here we demonstrate fully self-aligned CNTFETs that include a gate-all-around (GAA) the nanotube channels—the ideal gate geometry for a 1D CNT. These GAA-CNTFETs have 30 nm channel lengths and exhibit n-type operation with high *on*-currents and good switching behavior that is explained by quantum transport (NEGF) simulations. This work is an important milestone showing that a technologically relevant self-aligned device can be realized with nanotubes.

Introduction

The era of scaling silicon field-effect transistors (FETs) to ever-smaller dimensions is coming to a close. Meanwhile, CNTFETs have been experimentally shown to provide superb low-voltage performance with channel lengths scaled into the sub-10 nm regime (1). However, while proven to be aggressively scalable, CNTFETs typically employ impractical gate geometries, often with the source/drain contacts completely overlapping the gate. Realizing a self-aligned CNTFET has been difficult since common reactive ion etching (RIE) cannot be used to anisotropically etch materials without destroying the nanotube. The few reports on CNTFETs with self-aligned gates required very thin contact/gate metals (< 10 nm) (2-3) and/or a device structure that cannot be scaled (4).

Achieving a self-aligned CNTFET that can be scaled to the 10 nm range is critical if nanotubes are to be considered for a future high performance logic technology. In this work, a simple approach has been developed for yielding gate-all-around CNTFETs with the gate self-aligned to the source/drain contacts, separated by a well-defined spacer. This new device structure is primarily enabled by the anisotropic wet etching of silicon to suspend CNT channels and apply the GAA.

Gate-All-Around Fabrication

As mentioned above, the difficulty of finding an anisotropic etch that will not also damage or remove the CNTs is one of the central challenges to realizing a self-aligned device. This obstacle is overcome by employing a wet etch of <110> silicon that is highly selective to certain crystal planes (5). In this work, aligned arrays of single-walled CNTs grown on quartz substrates are transferred to silicon-on-insulator (SOI)

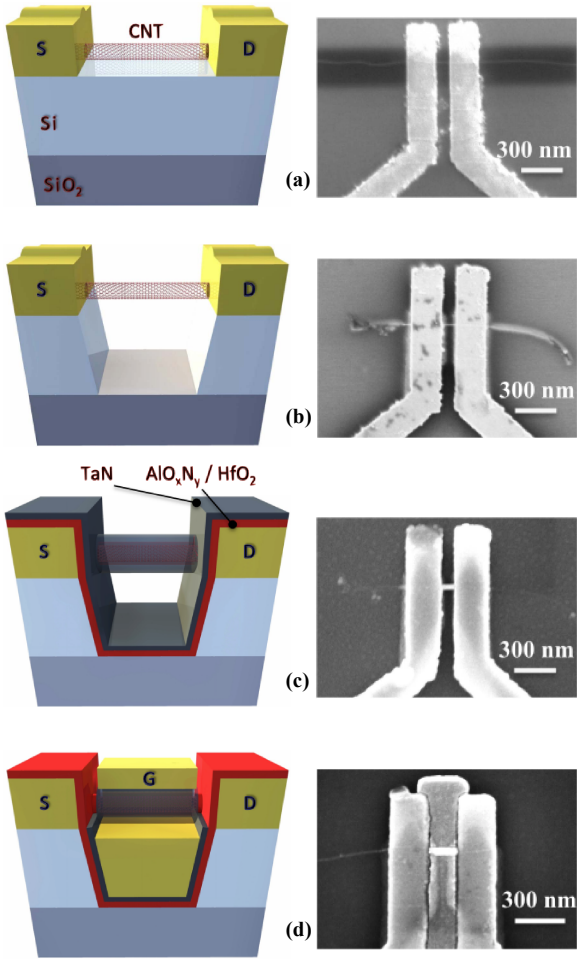

Figure 1. Process flow for fabricating self-aligned, gate-all-around CNTFETs; each step is illustrated with a cross-sectional schematic and corresponding top-view SEM image. (a) CNTs placed on SOI substrate and Pd source/drain contacts formed. (b) Anisotropic wet etch of Si in KOH causing CNT channel to be suspended. (c) Gate dielectric and metal deposited on CNT channel using ALD. (d) Self-aligned gate contact formed and TaN cleared from field.

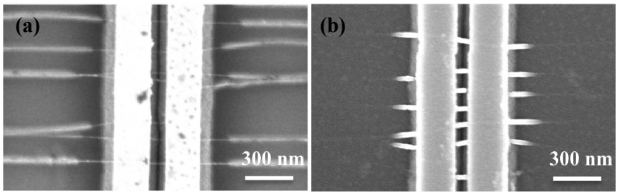

Figure 2. Top-view SEM images (a) after Si etch and (b) after ALD of gate-all-around dielectric and metal. Note how the CNTs are suspended between the metal contact lines in (a) and touch the substrate further away from the contacts. Likewise, only the suspended portion of the CNTs are annularly coated and thus visible in (b).

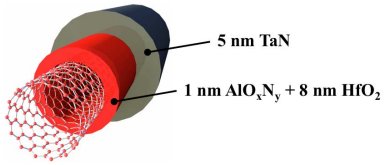

Figure 3. Illustration of the gate-all-around stack consisting of an annularly coated high-k dielectric and conductive TaN gate metal.

substrates with a <110> Si thickness of 55 nm. Next, electron beam lithography and metal deposition/lift-off are used to define Pd source/drain contacts (Fig. 1a). The contacts provide an etch barrier to protect the Si beneath as the Si in the channel area is removed in 30 wt. % KOH heated on an 80 °C hotplate, yielding suspended CNTs (Fig. 1b, 2a). The suspended nanotube channel enables a GAA approach and eliminates the adverse impact of stray charge and/or adsorbed molecules, which are typically found on oxide surfaces used to support CNTs. This isolation of the nanotubes from surface charges is significant considering the major role that such charges play in the observed variability of CNTFETs (6); hence the GAA approach provides an ideal platform for eliminating the variation in CNT devices so long as a high quality gate dielectric is employed.

Atomic layer deposition (ALD) is used to coat the suspended CNTs with a gate dielectric and metal. Because typical ALD precursors will not nucleate on sp^2 carbon, an adhesion layer of ~1 nm AlO_xN_y is deposited at room temperature followed by an anneal at 300°C overnight, then 8 nm HfO_2 dielectric at 125°C and finally 5 nm TaN at 250°C. A similar ALD adhesion layer was used in the only previous report of a GAA-CNTFET (7), but the device structure proved problematic as it relied on the isotropic wet etch of the gate dielectric/metal to define the channel, yielding poor transistor performance. After ALD, the resulting GAA-CNT stack is illustrated in Fig. 3 and is shown for an array of nanotubes in Fig. 2b.

The scanning electron microscope (SEM) image in Fig. 2a shows how the CNTs extend out from underneath the Pd source/drain contacts (vertical bars) and drape down to touch the substrate approximately 200 nm from the contact edge (the nanotubes appear thicker and brighter where they touch

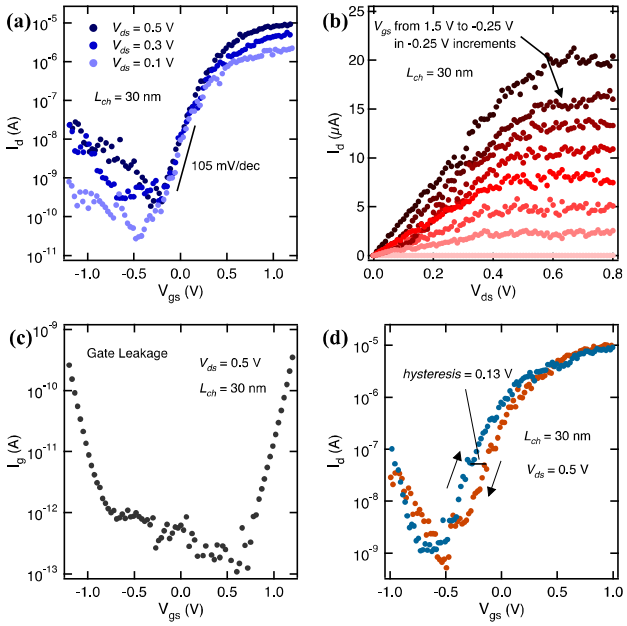

Figure 4. Characteristics of fully self-aligned GAA-CNTFET having a single nanotube channel with $L_{gate} \approx 30$ nm. (a) Subthreshold curves showing good switching behavior. (b) Output curves exhibiting saturation at ~0.45 V and high on-current (~20 μA at $V_{gs} - V_{th} = 1.25$ V). (c) Gate leakage indicating stable operation up to ~1.3 V. (d) Double sweep subthreshold curves showing small hysteresis in the device.

the substrate due to charging). After ALD of the dielectric and metal, the suspension of the nanotube channels can be seen even more clearly, with each CNT now wrapped in the GAA once it is off of the supporting substrate (suspended).

With the TaN GAA metal formed with ALD to ensure annular coverage, a final Pd gate electrode is established to contact the TaN. While designed with a slight gate overlap, the depth of the Si trench in the channel causes the gate electrode to be selectively removed from the source/drain during lift-off, as confirmed by atomic force microscope imaging. This process works even with a 50 nm thick gate electrode and yields a gate edge that mirrors the line-edge-roughness of the source/drain contacts (Fig. 1d). With the gate electrode covering the GAA-CNT channel, the unprotected TaN is removed using RIE. The result is a fully self-aligned GAA-CNTFET (Fig. 1d).

Self-Aligned 30 nm Channel GAA-CNTFET

Characteristics of a self-aligned GAA-CNTFET with a channel length (L_{ch}) of 30 nm are given in Fig. 4. The device contains a single CNT channel that exhibits a high *on*-current of ~16 μA at $V_{gs} - V_{th} = 1$ V with a peak transconductance of ~45 μS and an inverse subthreshold slope (*SS*) of ~105 mV/dec. This *SS* is slightly larger than expected for an ideal GAA owing in part to the sizable electron tunnel barriers that result from using high work function metal (Pd) contacts for

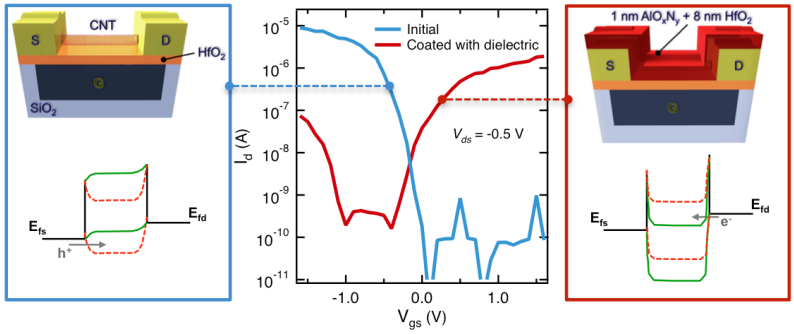

Figure 5. Subthreshold curves from same bottom-gated CNTFET before/after coating with dielectric stack that was used for the GAA devices. As illustrated in the band diagrams (green bands and red bands depict *on*-state and *off*-state, respectively), the GAA dielectric contains strong positive fixed charge that acts as doping across the CNT channel, converting the device from a p-FET to an n-FET.

an n-FET (see Fig. 5). All GAA-CNTFETs with this dielectric stack operate as n-FETs despite the use of high work function Pd contacts. This polarity shift is attributed to positive fixed charges in the HfO_2.

To validate the hypothesis of positive fixed charge in the dielectric causing the device n-FET operation, separate CNTFETs with bottom gates (nanotube channels exposed) were initially tested and then coated with the same dielectric stack as used in the GAA devices. The result, shown in Fig. 5, was a polarity shift from p-type to n-type along with a reduction in *on*-current (carriers now tunneling through barriers) and a higher *SS*. This insight helps put into perspective the comparatively much lower *SS* of the GAA-CNTFET (*i.e.*, the *SS* of the GAA is actually quite low considering the deleterious impact of the Schottky tunnel barriers and should be able to be significantly reduced).

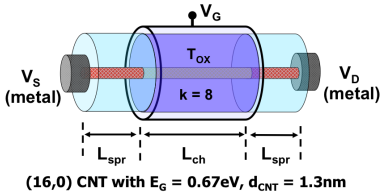

Figure 6. Schematic of GAA-CNTFET structure used in NEGF simulations. The spacers (L_{spr}) are the same dielectric and thickness as the gate dielectric in the experimental devices. A fixed charge density (N_d) is applied across the channel to represent the fixed charge from the ALD dielectric.

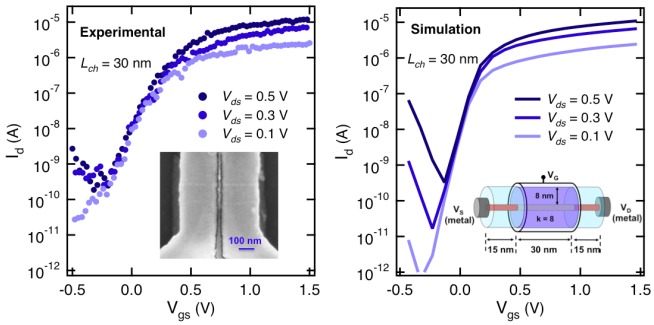

Figure 7. Comparison of experimental characteristics with NEGF simulation that approximates the device structure, including a fixed charge density $N_d = 0.4$/nm.

Discussion and Simulation of GAA-CNTFET

While self-alignment was achieved in the demonstrated device by taking advantage of the selective removal of the gate electrode from the top of the source/drain contacts during lift-off, this structure lends itself to more practical methods for achieving self-alignment. Most scalable is the approach of overfilling the trench-portion of the channel, as well as the rest of the chip, with a blanket of metal such as tungsten. Then, the tungsten can be chemical mechanical polished (CMP) back to yield the self-aligned device illustrated in Fig. 1d.

Self-consistent non-equilibrium Green's function (NEGF) formalism was used to model the GAA-CNTFET (8) with the parameters shown in Fig. 6. Selecting an appropriate fixed charge density (N_d) to represent the charges in the HfO_2 provided a reasonable comparison to the experimental data, as shown in Fig. 7. One key aspect of the present device is the spacers between the GAA and source/drain. These spacers are the same as the gate dielectric stack because they are formed when the dielectric is established using ALD. The impact of the spacer length (L_{spr}) on the subthreshold performance is shown in Fig. 8—the wider the spacer, the lower the *off*-current leakage. Spacer length in the

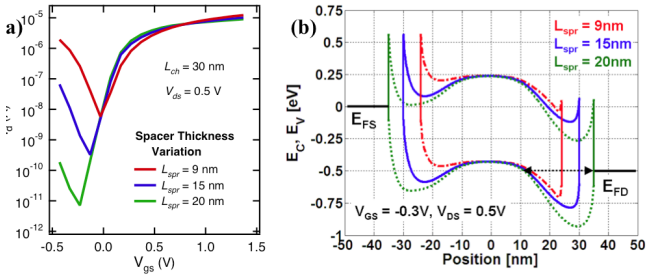

Figure 8. Simulation results showing the impact of the spacer thickness on the operation of a GAA-CNTFET with $N_d = 0.4$/nm. (a) Subthreshold curves showing a decrease in *off*-state leakage as the spacer thickness is increased. (b) Corresponding band diagrams illustrating the thinning of the tunnel barrier at the drain-end that causes more ambipolar leakage in thinner spacer devices.

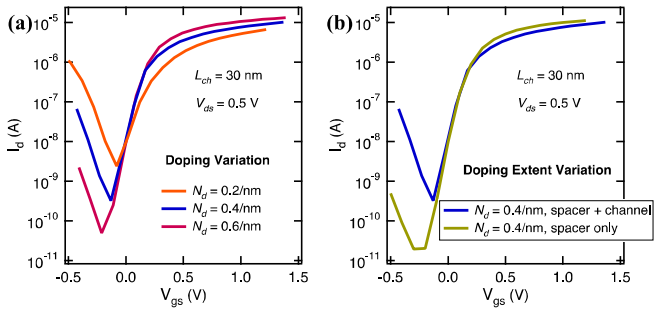

Figure 9. Simulation results of the impact of fixed charge doping concentration on the operation of a GAA-CNTFET with L_{spr} = 15 nm (gate metal work function has been adjusted in each case in order to obtain iso-leakage at V_{gs} = 0 V). (a) Subthreshold curves showing decreasing *off*-state leakage as doping is increased, enabled by wider tunnel barriers at the drain-end. Higher fixed charge density also shows higher *on*-currents from thinner tunnel barriers for source-injection. (b) Comparison of a device with the spacers and channel region both doped versus a device with doping only in the spacers. This more idealized structure yields a lower *off*-current and *SS*, with higher *on*-current.

experimental devices is between 9 and 15 nm based on the depth of the TaN GAA metal etch depth.

Another key aspect of these n-type GAA-CNTFETs is the density of fixed charge that is causing the device polarity shift. As shown in Fig. 9a, at a given L_{spr}, higher charge density in the dielectric creates larger tunnel barriers at the drain yielding lower *off*-currents; on the other hand, it also provides *thinner* tunnel barriers for source injection, thus leading to higher *on*-currents. However, such charge density can prove difficult to control. A more optimal scenario would be one that isolates the charges to the spacer regions, keeping the channel intrinsic. With this approach, the *off*-current is further reduced while correspondingly increasing the *on*-current (Fig. 9b)—higher gate work functions necessary for V_{th} adjustment in the case of CNTs with uniform dielectric charge also lead to depletion effects in the spacer regions that degrade overall performance.

Conclusion

This first demonstration of self-aligned CNTFETs that incorporate a completely surrounding gate delivers a high *on*-current device with good switching behavior. Focus in this paper is on an n-type device, which are historically more challenging to achieve for CNTs, but p-type GAA-CNTFETs are accessible in the same structure simply by using a dielectric that does not contain fixed charge. This work proves that the ideal gate geometry for CNTs is not only accessible, but also able to be realized in a technologically relevant self-aligned device.

Acknowledgements

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