Sub-10 nm Carbon Nanotube Transistor

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Within the next decade, transistors will be required with channel lengths (L_{ch}) below 10 nm—a length scale at which bulk-Si devices cannot perform. Single-walled carbon nanotubes (CNT) have been promoted as a replacement for Si owing to their superior electrical properties and ultrathin body. However, the feasibility of a high-performance, sub-10 nm nanotube channel without detrimental short-channel effects has been uncertain, with limited theoretical studies and no experimental evidence. Here we show the first sub-10 nm CNT transistor, which outperforms the published best competing Si-based devices with more than four times the current density (2.41 mA/μm) at a low operating voltage of 0.5 V. The transistor exhibits an impressively small inverse subthreshold slope (*SS*) of 94 mV/dec—nearly half of the value expected from a previous theoretical study. The superior low-voltage performance of sub-10 nm CNT transistors proves the viability of nanotubes for future aggressively scaled transistor technologies.

Device Fabrication

In a 200 mm wafer fab, metal local bottom gates capped with a 3 nm HfO_2 gate dielectric (equivalent oxide thickness, EOT ≈ 0.65 nm) were fabricated (Fig.1). Nanotubes were transferred onto the gates followed by a two-step source/drain metallization to form transistors with L_{ch} ranging from sub-10 nm to greater than 300 nm on the same CNT (Fig. 2-3). Scanning electron microscope (SEM) and transmission electron microscope (TEM) images in Fig. 1b-d portray the device structure. Especially significant is the cross-sectional TEM image in Fig. 1c that shows the sidewall shape of the source/drain contacts to ensure that channel length definition is accurate when measured from a top-view SEM image (*i.e.*, TEM image ensured that the metal does not slant inward, exaggerating the smallness of the channel length in top-view).

9 nm Channel Length CNT Transistor

Subthreshold curves of four transistors with L_{ch} from 320 nm down to 9 nm are given in Fig. 4. All of the curves are taken at the same drain-source bias (V_{ds}) of 0.4 V, yet there is an increase in the minimum current as L_{ch} decreases—a result of carriers tunneling through the channel energy barrier. Importantly, the *on*-current level for the three devices that have $L_{ch} \leq 41$ nm is consistent (if the curves are shifted on top of each other) and is evidence of reaching ballistic channel transport (negligible channel resistance) as shown in previous work [1].

Characteristics of the 9 nm channel length device reflect superb switching behavior in the *off*-state (Fig. 5a) and clear current saturation at a low V_{ds} of -250 mV in the *on*-state (Fig. 5b). The *SS* of 94 mV/dec is nearly half of the *SS* ≈ 170 mV/dec predicted by previous theory [2]. Further characterization of the devices is in Fig. 6-8. Importantly, these transistors are on a relatively large diameter CNT ($d_{CNT} \approx 1.3$ nm +/- 0.2 nm, band gap $E_g \approx 0.62$ eV +/- 0.1 eV); thus, a considerable reduction in *SS* and *off*-current at minimal cost to I_{on} is attainable by using smaller diameter nanotubes [1].

By numerical modeling of a single, bottom-gate CNT transistor that includes gate modulation of charge concentration in the source and drain contacts—an effect that is incorporated because the source and drain overlap the gate in these devices—a good fit to the 9 nm device subthreshold behavior is obtained (Fig. 9). Further work on transport physics at the contacts in these scaled devices must be pursued for a complete understanding of the many effects that impact scaling.

Comparison to Best Si-based Devices

To show the potential of using CNTs to replace Si for sub-10 nm transistor technologies, the scaling behavior is compared to three of the most advanced Si-based devices: nanowires with gate-all-around configuration [3], fins [4], and extremely thin Si on insulator (ETSOI) [5]. Each of the references reports the highest performing sub-10 nm gate length device of its type. As seen in Fig. 10, the scaling trend for the CNT transistors is similar to those reported for ETSOI and Si nanowires.

Future technologies will require operation at voltages at or below 0.5 V to limit power consumption. To compare the CNT transistor with the Si-based devices at a supply voltage ($V_{dd} = V_{ds} = V_{gs}$) of 0.5 V, a threshold voltage (V_{th}) of 0.2 V was assumed for all devices and then the *on*-current (I_{on}) was extracted from the reported data at a gate overdrive $|V_{gs} - V_{th}|$ of 0.3 V. As shown in the yellow column of the Fig. 10 table, the 9 nm nanotube device carries a diameter-normalized 2410 μA/μm while the best Si-based device reaches only 470 μA/μm (also diameter-normalized).

While normalizing the *on*-current by diameter is the most common method, it is not a practical projection. To be considered for a technology, CNTs must be densely packed at a certain pitch (as will nanowires and fins), so it is more realistic to consider the *on*-current normalized by a projected tube/wire/fin pitch. For nanowires and fins there must be room for the wire width and gate stack in the pitch, which is aggressively projected to be 20 nm, yielding 300 and 138 μA/μm for nanowires and fins at $V_{dd} = 0.5$ V, respectively. With a diameter of ~1 nm and no top gate stack, a pitch of 5 nm is projected for CNTs (200 CNTs/μm), which yields 630 μA/μm at $V_{dd} = 0.5$ V—still more than double the current in the best Si device.

Conclusion

This first demonstration of CNT transistors with channel lengths down to 9 nm shows substantially better scaling behavior than theoretically expected. Numerical simulations suggest that a possible explanation for the surprisingly good performance is a result of the gate modulating both the charge in the channel and in the contact regions. The unprecedented performance should ignite exciting new research into improving the purity and placement of nanotubes, as well as optimizing CNT transistor structure and integration. Results from aggressively scaling these molecular-channel transistors exhibit their strong suitability for a low-voltage, high-performance logic technology.

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[3] M. Li, *et al.*, *VLSI Tech. 2009 Symp.*, p. 94, 2009.
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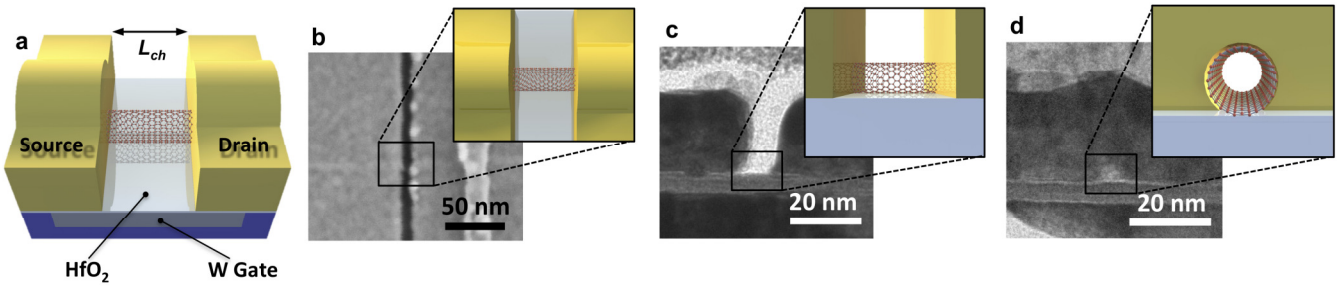


Figure 1. Sub-10 nm carbon nanotube transistor configuration with electron microscope images. (a) Schematic showing the local bottom gate device structure, with W gate, 3 nm HfO_2 dielectric, and Pd source/drain contacts. The channel length (L_{ch}) is indicated. (b) Top-view SEM image of ~9 nm channel length CNT transistor. This top-view was crucial because the line edge roughness of the contacts was such that the channel length was dependent on where the nanotube actually interfaced with the source and drain. (c) Cross-sectional TEM image showing the profile of the source/drain contacts to ensure accuracy of channel length definition. (d) Cross-sectional TEM image in the Pd contact area showing the metal covering a CNT, which is resting directly on the gate dielectric.

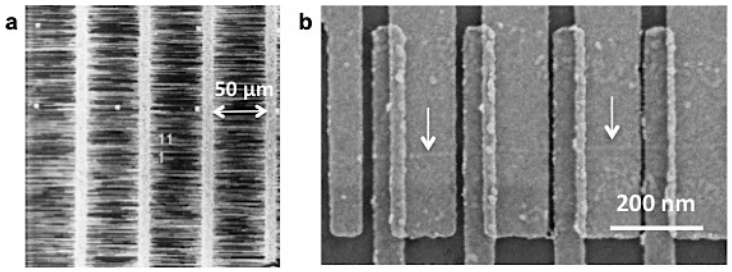


Figure 2. (a) SEM image of aligned CNTs after transfer onto substrate with local bottom gates. CNTs are ~50 µm long, extending from one catalyst stripe (bright, vertical line) to another. (b) SEM image of a set of devices on a single CNT (arrows indicate CNT location) showing how the staggered (offset in 10 nm increments) source/drain contacts enable a variety of channel lengths, including sub-10 nm.

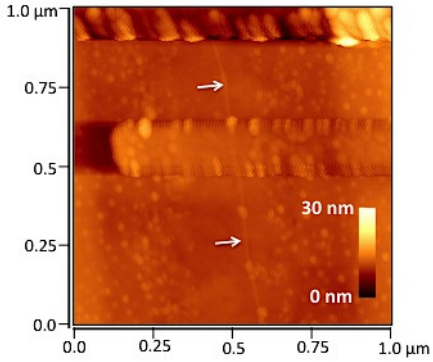


Figure 3. Atomic force microscope image of the nanotube used for diameter extraction. Average diameter was obtained from several such images.

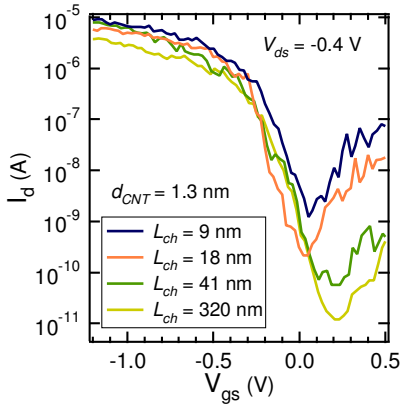


Figure 4. Subthreshold curves from four transistors assembled on the same CNT, showing increase in minimum current as L_{ch} is reduced and only mild degradation of *SS*. Having used the same nanotube for all channel lengths was critical because the energy band gap (E_g) for a CNT is inversely proportional to the diameter (d_{CNT}).

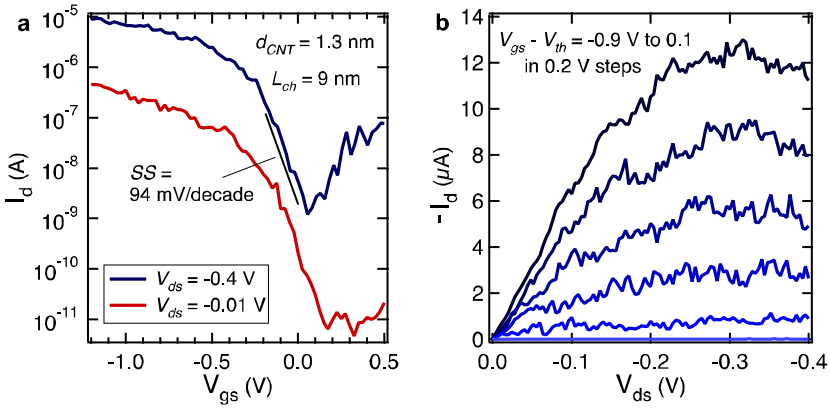


Figure 5. Characteristics of a 9 nm channel length CNT transistor. (a) Subthreshold characteristics (*off*-state) showing excellent switching behavior. The presence of hysteresis in the devices (see Fig. 8) is substantial enough to inhibit extraction of drain-induced barrier lowering (DIBL). (b) Output characteristics (*on*-state) at different gate overdrive ($V_{gs} - V_{th}$) conditions.

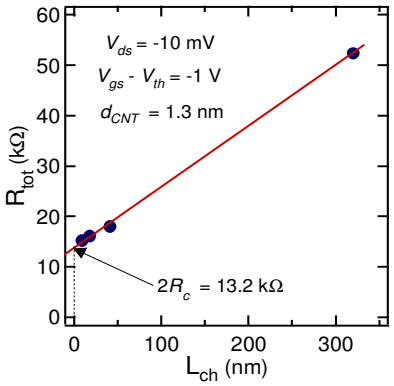


Figure 6. Transfer length model plot for the CNT used in the study. Total resistance (R_{tot}) is extrapolated to zero channel length to obtain the contact resistance, which is comparable to similarly contacted devices in a previous report [1].

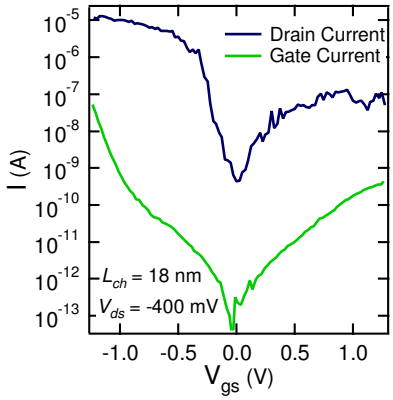


Figure 7. Drain and gate currents for the 18 nm channel length device showing the operating range for the 3 nm HfO_2 to be $|V_{gs}| < 1.2$ V. The large gate current is a result of the source/drain contacts overlapping the gate in the present devices.

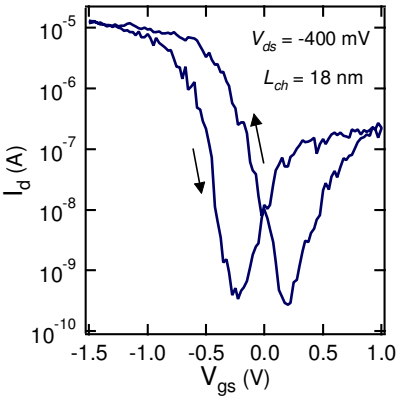


Figure 8. Gate voltage sweep from -1.5 V to 1.0 V and back on 18 nm channel length device, yielding hysteresis of 375 mV. With the CNT channel exposed to air, adsorbates such as water and oxygen act as mobile charge traps and induce the hysteretic behavior.

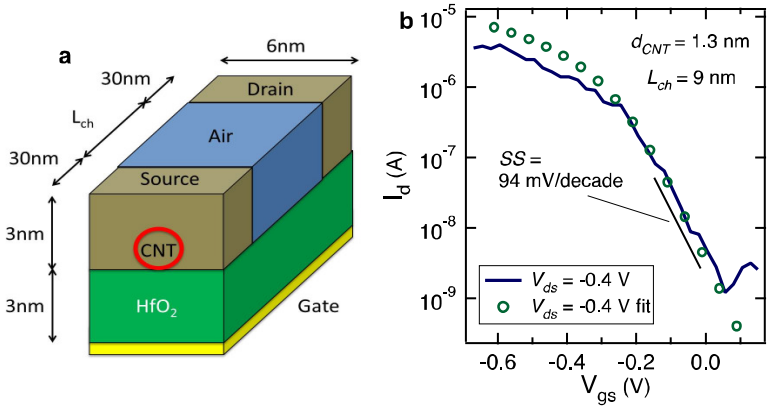
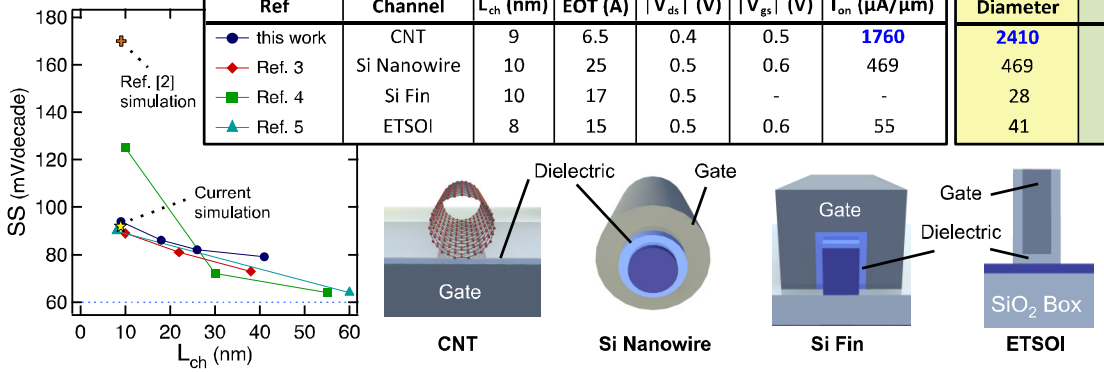


Figure 9. (a) Schematic of structure used in simulation (E_g = 0.65 eV), including doped source/drain contacts that are modulated by the overlapping gate. (b) Results from the NEGF numerical simulation plotted with the experimental subthreshold curve. Switching behavior matches very well, showing that further understanding of transport physics under contacts is vital for more accurate device modeling. Mismatch in the *on*-current is attributed to a difference in series resistance.



Ref	Channel	L_{ch} (nm)	EOT (Å)	$\|V_{ds}\|$ (V)	$\|V_{gs}\|$ (V)	I_{on} (μA/μm)	V_{dd} = 0.5 V I_{on} (μA/μm) Diameter	Pitch
this work	CNT	9	6.5	0.4	0.5	**1760**	**2410**	**630**
Ref. 3	Si Nanowire	10	25	0.5	0.6	469	469	300
Ref. 4	Si Fin	10	17	0.5	-	-	28	138
Ref. 5	ETSOI	8	15	0.5	0.6	55	41	41

Figure 10. Plot of the inverse subthreshold slope versus channel/gate length for CNT transistors compared to the best competing Si-based, n-type devices. Orange plus sign data point is from theoretical projection in reference [2]; yellow star data point is from current theoretical simulation showing significantly improved fit to sub-10 nm device; blue dotted line is thermal limit for *SS*. Table extended from legend compares other performance metrics for the sub-10 nm devices. White and yellow column I_{on} is normalized by diameter for CNT and Si nanowires and by two times fin height for Si fin. Green column I_{on} is normalized by physical pitch (spacing from one tube/wire/fin to the next), estimated to be 5 nm for CNTs and 20 nm for nanowires and fins. Yellow and green columns are performance at V_{dd} technology of 0.5 V, assuming ability to achieve threshold voltage (V_{th}) of 0.2 V for all devices with $|V_{gs} - V_{th}| = 0.3$ V used for I_{on} extraction. Cross-sectional schematics show the different gating configurations.