Can Carbon Nanotube Transistors be Scaled Without Performance Degradation?

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Abstract

The effects of channel length scaling on carbon nanotube field-effect transistor (CNTFET) performance was investigated by varying device lengths on the same nanotube. Results show that scaling improves performance with substantial increases in on-current, resistances closer to the quantum limit than have ever been reported, and the shortest (~30 nm) well-behaving CNTFETs to date.

Introduction

While there have been many demonstrations of carbon nanotube field-effect transistors (CNTFETs) performing beyond projected Si technology, there remain important questions about CNT devices that must be answered before their large scale integration is considered. One question is: Can CNTFETs be scaled without losing their impressive performance? Previous reports of scaled CNTFETs have either shown severe short channel effects or employed device geometries that limit aggressive scaling [1, 2]. One of the best performing devices to date was limited by a minimum dielectric thickness of 8 nm and a maximum contact metal thickness of 7 nm [2]. Furthermore, variation in nanotube diameter and device geometry among reports has made it unfeasible to reach any conclusions regarding CNTFET scalability.

We have investigated the direct effects of channel length (L_g) scaling on CNTFET performance by fabricating different L_g devices on the same CNT. Our results show a consistent increase in on-current (I_{on}) by up to two times with no short channel effects when scaling L_g from > 140 nm down to ~30 nm on the same CNT. Furthermore, we confirm ballistic transport in an L_g = 38 nm device, with $I_{on} \approx 18$ µA and an I_{on}/I_{off} ratio > 10^5. Not only do these CNTFETs outperform similar devices, but they do so using small diameter CNTs ($d_{CNT} \leq 1.2$ nm), compared to the typical $d_{CNT} \geq 1.7$ nm. This is an important advancement considering the CNT band gap is inversely proportional to d_{CNT} ($E_G \approx 0.8$ eV/d_{CNT} nm).

Device Structure

Several devices with different L_g's were fabricated on the same CNT to obtain a fair comparison of the scaling effects. Details of the device structure are shown in Fig. 1. A local bottom gate (LBG) geometry was used and provides several advantages for CNTFETs, including flexibility in gate metal options and ability to use ultrathin dielectrics. The LBG is nearly level with the surrounding SiO_2 to avoid distorting or bending the nanotube. Source and drain contacts were deposited directly onto the intrinsic CNT channel, forming Schottky barrier (SB) type FETs. Pd contacts (15 nm thick) were used to obtain the lowest possible SB for p-channel transport. All devices used CNTs from a laser ablation source (average $d_{CNT} \approx 1$ nm) [3].

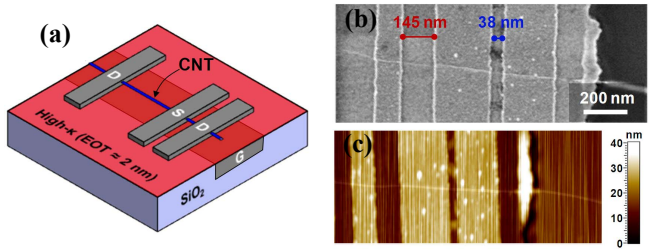

Figure 1. (a) Schematic, (b) scanning electron microscope (SEM), and (c) atomic force microscope (AFM) images showing a semiconducting CNT on top of an LBG (Pd), with Pd electrodes forming two different channel length devices. The dielectric is 10 nm HfO_2 with $\kappa \approx 18$, yielding an EOT ≈ 2 nm. AFM was used to determine the CNT diameter, $d_{CNT} \approx 1.2$ nm.

While 10 nm of atomic layer deposited HfO_2 (EOT ≈ 2 nm) was used herein, the LBG geometry enables aggressive dielectric scaling, limited only by the roughness of the metal gates. In a top-gate geometry, at least 8 nm of dielectric must be deposited in order to completely cover the CNT because the dielectric will not nucleate on the nanotube itself [2]. To overcome this limitation, CNTs can be chemically or molecularly functionalized, forcing a dielectric to coat them; but such functionalization can lead to degraded transport properties [4, 5]. Therefore, the LBG geometry provides a solution to scaling dielectrics without CNT functionalization.

Effects of Scaling

The primary discussion herein will be for a semiconducting CNT (shown in Fig. 1) with a diameter of ~1.2 nm ($E_g \approx 660$ meV). Characteristics in Fig. 2 are from an L_g = 38 nm device and show the shortest well-behaving CNTFET to date. A subthreshold slope (*SS*) of 94 mV/dec is extracted, which is quite close to the ideal 60 mV/dec despite the presence of SBs. The ultrathin 1D CNT body and scaled gate dielectric (EOT ≈ 2 nm) ensure that the SBs are extremely thin (essentially transparent to carriers). The current is mostly limited by thermionic emission over the barrier inside the channel—a mechanism similar to conventional MOSFETs. As mentioned above, the novel LBG geometry will allow more aggressive dielectric scaling, further helping the current injection. Compared to CNTFETs with similar d_{CNT} from a variety of device geometries, the I_{ds} of ~18 µA at V_{ds} = -0.5 V is several times greater than has been observed [3], owing to both the smaller L_g and improved gating electrostatics. The output characteristics (Fig. 2b) show low total resistance (R_{tot}) at low biases and good current saturation at high biases.

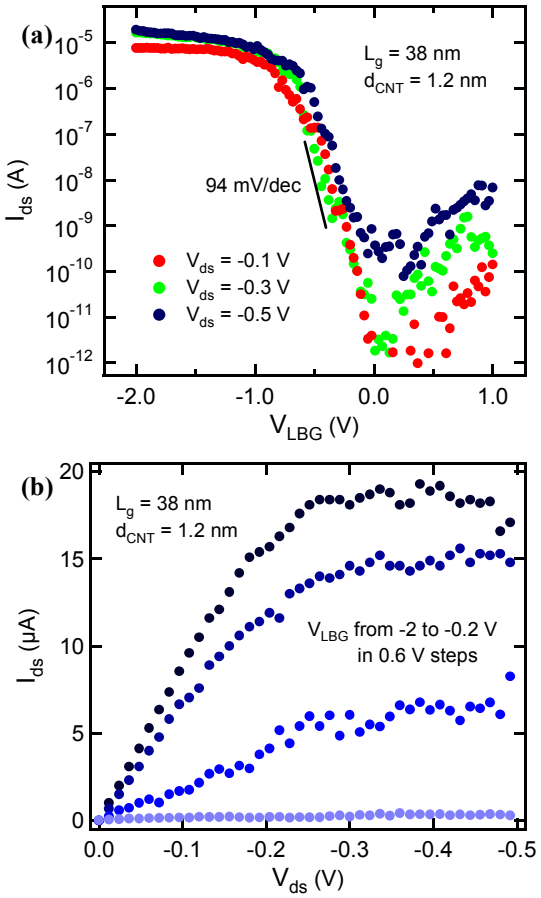

Figure 2. Characteristics of L_g = 38 nm device from a CNT with $E_g \approx 660$ meV. (a) Subthreshold plot for different V_{ds} with $SS \approx 94$ mV/dec; note that the slight shift in V_{th} between the curves is attributed to hysteresis caused by testing the devices in air and without passivation. The V_{th} is also shifted because of the high work function (~ 5.2 eV) Pd gate. (b) Output curves for different V_{LBG} showing good saturation and on-current of ~13 μA at 0.5 V overdrive (V_{LBG} - V_{th} = V_{ds} = -0.5 V). There was no detectable gate leakage current in any of the devices presented herein.

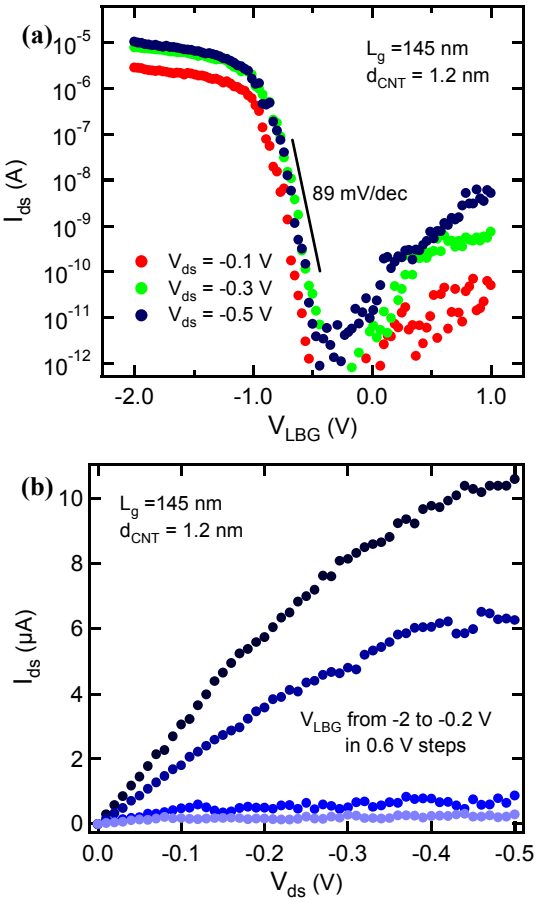

Figure 3. Characteristics of L_g = 145 nm channel device from the same CNT as in Fig. 2. (a) Subthreshold plot for different V_{ds} with $SS \approx 89$ mV/dec. (b) Output curves for different V_{LBG} showing the beginning of saturation and current of ~7 μA at 0.5 V overdrive (V_{LBG} - V_{th} = V_{ds} = -0.5 V).

To verify that the excellent behavior of the L_g = 38 nm device can be attributed to scaling, characteristics from a CNTFET with L_g = 145 nm on the same CNT are given in Fig. 3. Note that the *SS* of 89 mV/dec is similar to that exhibited by the 38 nm device (94 mV/dec). In fact, a third device with L_g = 450 nm was fabricated on this same CNT (characteristics not shown) and had a *SS* of 96 mV/dec, clearly indicating that the scaled L_g is not adversely impacting the channel electrostatics. Note that there is a slight difference in the threshold voltage (V_{th}) between the devices; however, this was not observed with other scaled CNTFETs in this study and is attributed to hysteresis caused by testing the devices in air. In fact, it is significant that these devices perform so impressively when tested in air and without passivation or annealing—comparable reports have suggested a 2-5 fold conductance increase after passivating and annealing CNTFETs [2].

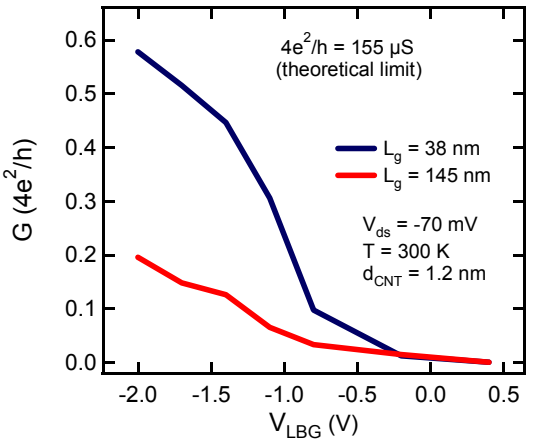

Figure 4. Conductance at room temperature for two different channel length devices on the same CNT, illustrating the clear advantage that scaling has for the on-state. The 38 nm device exhibits the highest conductance ever reported for a semiconducting CNT that has a demonstrated $I_{on}/I_{off} > 10^2$ (present device has $I_{on}/I_{off} > 10^5$).

A comparison of the conductance at room temperature for the two different L_g devices is given in Fig. 4. The quantum conductance (resistance) for CNTs is $G_o = 4e^2/h \approx 155\ \mu S$ (~6.5 kΩ), and the 38 nm device exhibits $0.58G_o$ at low bias; to our knowledge, this is the highest room temperature conductance from a CNTFET that has been reported—an advancement made more significant by the fact that it was achieved using a small diameter nanotube (~1.2 nm). The best performing CNTFETs typically employ larger d_{CNT} nanotubes (≥ 1.7 nm) to obtain lower SB heights [1-3]; however, in CNTs the band gap is inversely proportional to d_{CNT}, leading to off-currents in large-diameter CNTs. The present devices exhibited on-currents comparable to large d_{CNT} devices while maintaining large I_{on}/I_{off} ratios. For the 145 nm device, the conductance of $0.2G_o$ is comparable to that of other reported devices with Pd contacts and $L_g > 100$ nm, with the exception that such devices use CNTs with $d_{CNT} \geq 1.7$ nm. Once again, the fact that similar conductance was achieved with a smaller diameter (larger band gap) CNT is evidence of good electrostatics in the LBG geometry allowing for thin SBs.

Verification of Ballistic Transport

One motivation for scaling is to reduce scattering from acoustic and optical phonons (AP and OP). Such scattering suppression is evident in the I_{ds} vs. V_{ds} and I_{ds} vs. electrical field (E) plots in Fig. 5. If diffusive transport were to be assumed, then the low-field slopes for the 38 and 145 nm devices should be the same in the inset I_{ds} vs. E plot ($v = \mu E$, μ = constant). However, in this case the smaller L_g gives lower dI_{ds}/dE slope at the same $V_{LBG}-V_{th}$. This counterintuitive result arises because the mobility is no longer constant with respect to L_g and indicates a transition from the diffusive to the ballistic transport regime. At higher fields, OPs become significant, causing the current to saturate; since the 38 nm device is much closer to the OP mean free path (l_{OP}), less scattering events take place and thus higher saturation currents are achieved.

To provide further confirmation of ballistic transport in these scaled CNTFETs, characteristics from devices of different length (L) on a single metallic CNT were obtained (Fig. 6). Studying transport in metallic nanotubes provides information on lattice scattering mean free paths that can be used as a baseline for understanding transport in semiconducting nanotubes where band gaps and SBs further complicate transport properties. A CNT was determined to be metallic when it displayed $I_{on}/I_{off} < 10$, indicating no band gap. Note in Fig. 6 how the current saturated readily at ~20 μA for the 300 nm long CNT device, whereas each of the shorter devices was able to reach increasingly larger currents before their conductance reduced. Using the conductance of the 15, 45, and 70 nm devices in the high-field region, l_{OP} is extracted from $G = G_o[l_{OP}/(l_{OP}+L)]$, with a consistent result of $l_{OP} \approx 15$ nm for each device, which is consistent with simulated transport studies [6]. The 15 nm long device

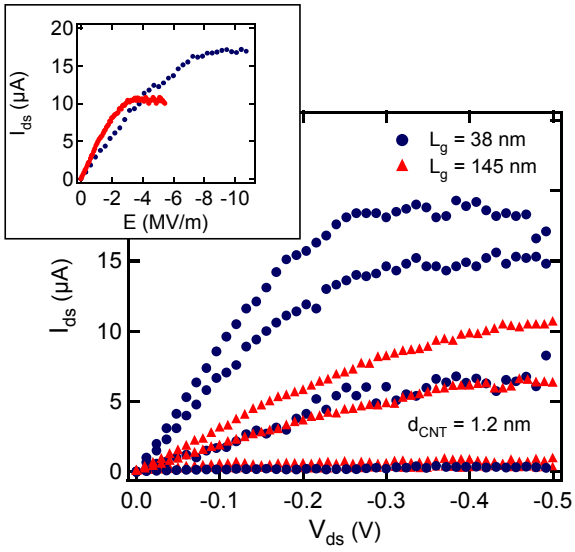

Figure 5. I_{ds} vs. V_{ds} for two different L_g devices on the same CNT at a range of V_{LBG}, showing a higher low-field slope for the 38 nm device. The upper inset is I_{ds} vs. electric field (E) at $V_{LBG}-V_{th}$ = -1.1 V for the same two devices. For a typical diffusive MOSFET μ is not length dependent (μ = v/E), but in the present case a smaller L_g decreases the slope at low fields. At higher fields, the increase in I_{ds} from the 145 nm (10 μA) to the 38 nm (~17 μA) device is attributed to lowered OP emission (l_{OP} ≈ 15 nm, extracted from Fig. 6).

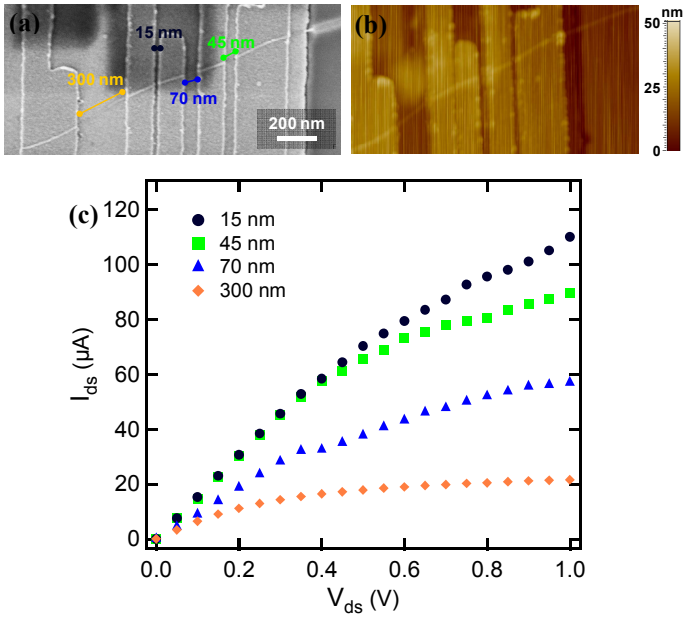

Figure 6. (a) SEM and (b) AFM images showing a metallic single-walled CNT on top of a LBG, with Pd electrodes forming four different length devices (confirmed metallic by observing $I_{on}/I_{off} < 10$). (c) Characteristics of the metallic CNT devices showing how scaling affects transport on the same metallic CNT. The 15 nm device exhibits a low-field resistance of 6.6 kΩ, which is the closest to the quantum resistance (~6.5 kΩ) that has been reported [6]. Both the 15 and 45 nm devices are ballistic, while the 70 nm device is quasi-ballistic.

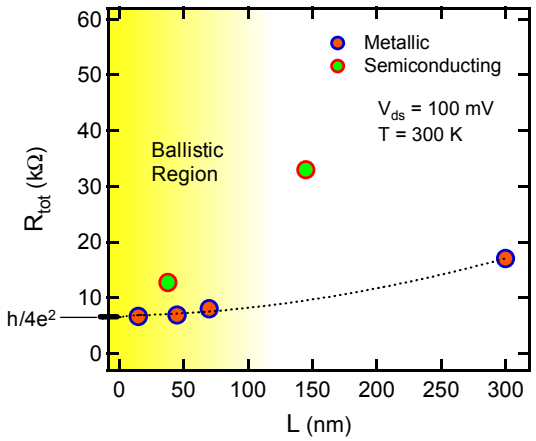

Figure 7. Resistance vs. channel length for two devices on the same semiconducting CNT (from Fig. 5) and four devices on the same metallic CNT (from Fig. 6). For the semiconducting CNT, R_{tot} values were taken at the same V_{LBG}–V_{th} = -1.1 V and V_{ds} = -0.1 V, and for the metallic CNT R_{tot} was taken from V_{ds} = 0.1 V. The traditional trend involves (starting from longer lengths) a linear diffusive transport regime (usually beginning near l_{AP}) with an eventual saturation of R_{tot} in the ballistic regime (these would be connected by a gradually sloping quasi-ballistic regime) [8]. The trend line on the metallic CNT devices illustrates the transition from the quasi-ballistic to the ballistic regime—transport is ballistic for the metallic CNT at 15 nm (~6.6 kΩ) and 45 nm (6.9 kΩ), with the trend clearly saturating at $1/G_o$. This metallic CNT trend helps confirm ballistic transport in the 38 nm CNTFET assuming transport at low fields is comparable between semiconducting and metallic CNTs. When moving towards the diffusive regime, however, transport between metallic and semiconducting CNTs has been observed to differ quite dramatically [8].

exhibited a low-field R_{tot} of 6.6 kΩ (152 μS ≈ $0.98G_o$), which is closer to the theoretical limit than has yet been observed [7], and is clearly indicative of ballistic transport. In fact, the low-field slopes for the 15 and 45 nm devices are nearly identical, suggesting that the 45 nm device has already entered the ballistic regime.

R_{tot} values from the semiconducting and metallic CNT devices are plotted versus length in Fig. 7. These resistance values were extracted at $|V_{ds}|$ = 100 mV for all devices, and at the same overdrive (V_{LBG}–V_{th} = -1.1 V) for the CNTFETs. The transition from quasi-ballistic to ballistic transport is clear for the metallic CNT, with the 15 and 45 nm devices saturating in the ballistic region [8]. As mentioned previously, a first order approximation is made that carrier transport at low fields for metallic and semiconducting CNTs is nearly the same at short lengths. Using this approximation, the metallic R_{tot} trend helps confirm that the 38 nm CNTFET is indeed ballistic. Therefore, the R_{tot} of 12 kΩ at V_{LBG}–V_{th} = -1.1 V for the 38 nm CNTFET consists of $1/G_o$ plus the resistance from the SBs. As length increases, the differences between metallic and semiconducting CNTs become greater, with effects such as charge pile-up becoming more significant in gate controlled CNTFETs, eliminating the benefits of any comparison [6, 8].

Conclusion

Scaling the channel length of devices on the same CNT has now provided clear evidence that CNTFETs not only retain their performance when scaled, but have several enhanced properties. By scaling L_g from 145 nm down to 38 nm, we observed no indication of short channel effects, a substantial increase in on-current, and ballistic transport with resistances closer to the quantum limit than have ever been reported. Thus, the answer to the question in the title is indeed, "yes." Furthermore, we demonstrated that the LBG geometry allows for CNTFETs with exceptional characteristics to be realized using small diameter CNTs ($d_{CNT} \leq$ 1.2 nm), outperforming comparable devices that employed $d_{CNT} \geq$ 1.7 nm.

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