Stacking Graphene Channels in Parallel for Enhanced Performance With the Same Footprint

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***Abstract*—Using the unique ability of graphene to be transferred to virtually any surface, field-effect transistors are demonstrated with vertically stacked graphene channels that are electrically connected in parallel. The graphene in each layer is double gated, with all gates in the stack connected to a common gate electrode. We show that the performance of these devices scales linearly with the number of stacked graphene channels at rates of approximately 500 μA/μm and 200 μS/μm per layer for the ON-current and peak transconductance, respectively. This demonstration reveals the ability to employ graphene in a novel fashion for tuning and amplifying the performance of a transistor without changing the device footprint.**

***Index Terms*—Double gate, field-effect transistor (FET), graphene, parallel channels, stacked.**

I. Introduction

GRAPHENE, while atomically thin, exhibits an extremely high mobility for both electrons and holes [1]. As a 2-D channel material, graphene has enabled high-frequency transistors, including integration into small radio frequency (RF) circuits such as a voltage amplifier [2] and a mixer [3]. The primary limitations to graphene transistor performance are related to degradation in carrier transport or injection caused by the needed gate dielectric and metal contact interfaces [4]. Most studies on graphene transistors have focused on improving these interfaces to maximize performance [5]–[9].

When graphene is grown on copper foil using chemical vapor deposition (CVD), it can be transferred to virtually any substrate, from plastic [10], [11] to silicon [2], [10]. This unique substrate independence makes possible the fabrication of devices that are not limited to a single active channel or layer in the way that devices fabricated from bulk materials are. In this study, we demonstrate the ability to amplify and tune the performance of graphene transistors by vertically stacking gated graphene channels that are electrically connected in parallel to common source and drain contacts. By using the same lithographic patterns/masks for each layer, a linear increase in the average ON-current and peak transconductance is demonstrated.

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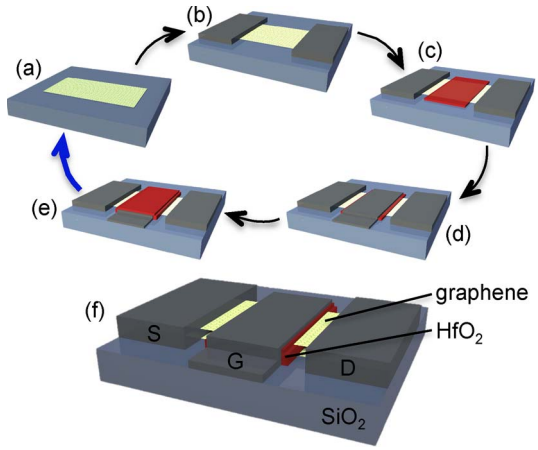

Fig. 1. Process for fabricating a FET with stacked graphene channels connected in parallel. Schematic of a device after (a) transfer and patterning of a graphene layer, (b) formation of Pd source and drain contacts, (c) patterned deposition and liftoff of HfO_2 gate dielectric using ALD, (d) formation of Pd gate, and (e) second patterned formation of HfO_2 gate dielectric. Steps (a) to (e) are repeated to form additional graphene layers, all connected in parallel. (f) Schematic of a stacked graphene transistor with two parallel graphene channels.

II. Device Fabrication

The process flow for fabricating each layer of a stacked graphene transistor is shown in Fig. 1. After CVD growth of the single-layer graphene on a Cu foil, the graphene is transferred to the device substrate and patterned to the desired size using electron beam lithography (EBL) of polymethylmethacrylate resist and oxygen plasma etching of the unwanted areas of graphene [see Fig. 1(a)]. Source and drain contacts are then patterned using EBL, followed by the electron beam evaporation of 30-nm Pd and liftoff in acetone.

To form the gate stack, the dielectric area is patterned using EBL followed by atomic layer deposition (ALD) of ~1-nm AlO_xN_y (ten cycles of NO_2, trimethylaluminum, and water vapor) at room temperature as an adhesion layer to the graphene [12] and, then, 10-nm HfO_2 (tetrakis(dimethylamido) hafnium and water vapor) at 125 °C for the dielectric. The schematic in Fig. 1(c) illustrates a device at this stage after liftoff in acetone. Next, a gate is established by EBL patterning followed by deposition and liftoff of 10-nm Pd. Finally, the same dielectric pattern is again written using EBL, and another ALD of the same dielectric stack is used to cover the gate metal, as shown in Fig. 1(e). With a gate stack thickness of approximately 32 nm (11-nm dielectric + 10-nm metal + 11-nm dielectric) and the source/drain thickness of 30 nm, the top surfaces of the device

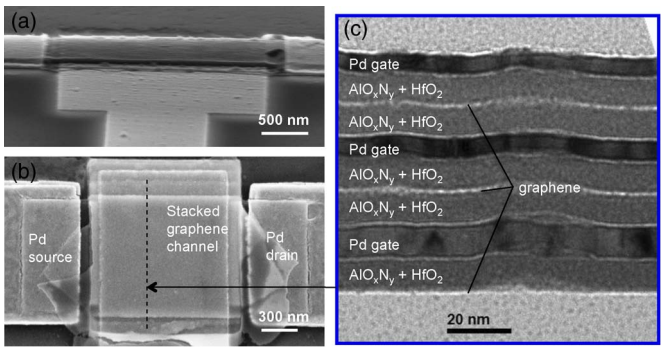

Fig. 2. (a) Tilted SEM image of a stacked graphene transistor with a 2.5-μm channel length and two parallel graphene channels. (b) Top-view SEM image of a device with three parallel graphene channels and a 1.5-μm channel length. (c) Cross-sectional TEM image of a three-layer stacked graphene channel identifying the different layers in the stack.

are nominally at the same height to provide a planar surface for the next graphene layer to be deposited.

All of these process steps are then repeated, using the same patterns (masks), to form as many vertically stacked layers as desired. Importantly, all of the source/drain contacts are shorted together, connecting all of the graphene layers in a device in parallel. The gate layers are also shorted together at a distance of 1 μm from the active channel. In the present case, the devices were electrically tested in air following the completion of each layer to study the changes in performance. A schematic of a device with two stacked layers is shown in Fig. 1(f).

III. Results and Discussion

Physical characterization of this unique transistor structure was done using scanning electron microscope (SEM) and transmission electron microscope (TEM) imaging. The SEM images of Fig. 2(a) and (b) show stacked graphene transistors from tilted and top views, respectively. In the SEM of Fig. 2(b), there are three stacked graphene layers, and a distinct indentation in the surface can be seen where the graphene is located in the source/drain and channel regions. To ensure the uniformity of the various layers in the gate stack, cross-sectional TEM images were taken, as shown in Fig. 2(c). These images confirm the high uniformity and consistency of the ALD dielectric thickness, and the three stacked graphene channels can be seen between the dielectric layers.

The quality of the graphene films after transfer was studied using Raman spectroscopy. Measurements from three different locations on a film posttransfer are given in Fig. 3(a) and show that a D-band is present in some areas and not others—evidence that the quality of the film is not homogeneous. We also obtained mobility data as a function of carrier density from multiple graphene sheets grown using the same process and transferred to Si substrates having 90-nm SiO_2 [see Fig. 3(b)]. Both Hall mobility and carrier density were determined by the standard Van der Pauw technique at room temperature. While a linear trend is suggested from the data, the difference in mobility among the films also suggests a range of difference in quality from film to film.

Transfer characteristics from a representative stacked graphene transistor are given in Fig. 4(a). These three curves

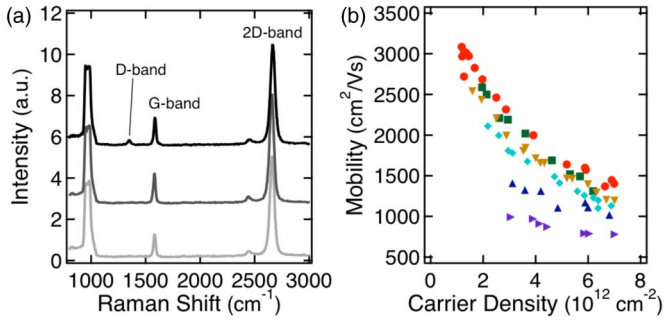

Fig. 3. (a) Raman measurements taken at 532-nm excitation from three different locations of a graphene film after transfer to the device substrate. (b) Hall mobility versus carrier density from several different graphene films from the same growth and transfer process.

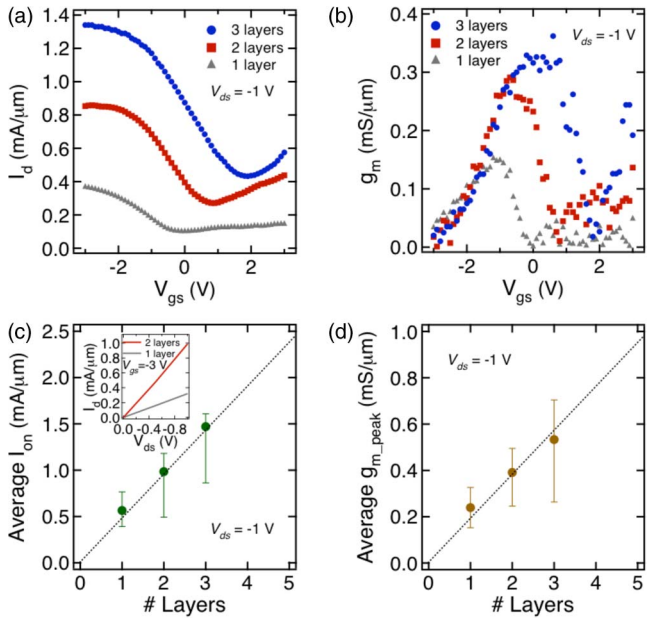

Fig. 4. (a) Transfer curves from the same device taken after the formation of each vertically stacked graphene layer. The channel length is 1.5 μm. (b) Peak transconductance from the same device as in (a). (c) Average ON-current (defined as I_d at $V_{\rm gs} - V_{\rm Dirac} = -2$ V) and (d) average peak transconductance for a set of 26 devices versus the number of stacked graphene layers in a device. The inset to (c) is a plot of the output characteristics from a device with a single and then a double layer. The dashed lines are a linear fit to the average data points, and the error bars represent the high and low values.

are from the same device as it was tested after the completion of each layer. The improved performance with each additional layer is evident in the transfer curves, along with a notable positive shift of the Dirac point $(V_{\rm Dirac})$ as layers are added. This shift is attributed to charge transfer of negative charge from the graphene caused by NO_2 exposure during the AlO_xN_y deposition, as has been observed for carbon nanotubes with the same sp^2 carbon surface [13]. The shift in $V_{\rm Dirac}$ is approximately 1 V for each stacked graphene layer and can be mitigated by employing a dielectric annealing step to drive off unwanted charge after each layer is deposited.

The transconductance (g_m) from the Fig. 4(a) device is plotted in Fig. 4(b). Since the primary application space for graphene transistors is RF electronics, g_m is perhaps the most crucial performance metric at the transistor level—the cutoff

and maximum frequencies are directly proportional to g_m. As seen in the Fig. 4(b) curves, g_m does increase with each stacked graphene layer, particularly closer to V_{Dirac}. However, further into the p-branch, away from V_{Dirac}, there is little to no improvement in g_m. This is a result of the large series resistance from the access, or ungated, regions between the gate and source/drain. These access regions are approximately 150 nm long in these devices, and as $V_{\mathrm{gs}} - V_{\mathrm{Dirac}}$ increases, the associated resistance of these regions comes to dominate transport in the device and thus prevents the transconductance from improving. Smaller access lengths or doping in these regions would help minimize their influence so that the g_m benefit could apply further into the ON state.

Average ON-current (extracted at $V_{\mathrm{gs}} - V_{\mathrm{Dirac}} = -2$ V and $V_{\mathrm{ds}} = -1$ V) and peak transconductance versus the number of stacked graphene layers from 26 devices are plotted in Fig. 4(c) and (d), respectively. A linear fit was added to each plot to show how the scaling behavior follows a linear trend, thus enabling the tuning of performance by selecting the appropriate number of layers. For each graphene layer, averages of $\sim 500\mu\mathrm{A}/\mu\mathrm{m}$ and $\sim 200\mu\mathrm{S}/\mu\mathrm{m}$ were added. Considering that these values were achieved at relatively long channel lengths of 1.5 μm, it is reasonable to expect that much better performance per layer is achievable. Most important from this study is that the performance is linearly increasing with each added layer.

Because these devices contain a double-gate structure for the graphene layers, the oxide capacitance C_{ox} will be increased compared to single-gate structures. For this reason, the maximum RF performance of these devices will be realized when they operate in the quantum capacitance C_q limit, where the total gate capacitance $C_g \approx C_q (C_q < C_{\mathrm{ox}})$. It has been shown that, with the appropriate gate dielectric, operation in the C_q limit is possible in graphene devices [14].

A final point regarding Fig. 4(c) and (d) is in relation to the rather large error bar range, which represents the high/low data points. These devices were fabricated using CVD-grown graphene, which takes on various defects in the transfer process. With 1.5-μm channel lengths, an inhomogeneous distribution of defects and domain boundaries is present in these devices, causing at least one and sometimes more than one of the layers to have poor performance. Decreasing the channel length and/or improving the quality of the graphene will tighten the distribution and improve the consistency.

IV. Conclusion

In conclusion, we have demonstrated that graphene channels can be vertically stacked in field-effect transistors (FETs) to control and enhance the ON-current and transconductance. Devices with up to three parallel graphene channel layers were demonstrated, showing a linear improvement of approximately 500 $\mu\mathrm{A}/\mu\mathrm{m}$ and 200 $\mu\mathrm{S}/\mu\mathrm{m}$ for each graphene layer added. This stacking of a 2-D material at the device level provides important insight into the unique device structures that are made possible by graphene.

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