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Consistently low subthreshold swing in carbon nanotube transistors using lanthanum oxide

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While a few singular reports have demonstrated carbon nanotube (CNT) transistors with subthreshold swings (*SS*) close to the theoretical limit (60 mV/decade), the majority of devices have more than double the target swing. Here, we show that a low temperature lanthanum oxide dielectric is able to yield a consistently and reproducibly low *SS*, with an average of 73 mV/decade and a low of 63 mV/decade. This LaO_x film is characterized using medium energy ion scattering and shown to be scalable down to 3.5 nm with minimal leakage and a variation in swing of only ±13%. With interface traps playing a dominant role in the switching behavior of CNT transistors, these results reveal the existence of dielectrics with more favorable interfacial characteristics for nanotubes that yield low *SS* devices. © *2013 American Institute of Physics*.
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Carbon nanotube (CNT) field-effect transistors (FETs) are touted for their ability to provide high-performance at low voltages. With recent reports of high performance devices scaled to sub-10 nm dimensions[1] and circuits that can operate at a mere 0.4 V,[2] the prospects for CNTFETs look promising. However, to completely deliver on the promise of a robust low voltage technology, CNTFETs must exhibit superb switching behavior in the form of a consistently low subthreshold swing (*SS*). *SS* is a measure of the amount of gate voltage (V_{gs}) needed to modulate the current (I_d) in a transistor by a factor of ten, or a decade (dec). While there have been a few reports showing a single device with *SS* very near the room temperature theoretical limit of 60 mV/dec,[3–5] the vast majority of reports show CNTFETs with more than double the desired *SS*.

Stray capacitance is the primary detriment to the switching behavior of a CNTFET. Carrier injection at the source contact can also limit *SS* under certain circumstances. For an intrinsic semiconductor FET like a CNTFET, the carriers must be injected into the channel from the source contact, most typically by tunneling through a Schottky barrier. Such tunneling will cause *SS* to increase when the thermal barrier in the channel is small and the device is close to the *on*-state. However, deeper into the *off*-state a Schottky barrier device will still be controlled by the thermal barrier in the channel. Furthermore, high work function metals such as Pd have been shown to yield CNTFETs with negligible Schottky barriers,[6,7] minimizing their impact. Stray capacitance is, therefore, the most dominant factor for determining *SS* in CNTFETs and is critically dependent on the choice of gate dielectric.

Because a CNT is intrinsic and consists of strong sp^2 bonded carbon, the only stray capacitance that is likely to impact *SS* is the interface trap capacitance (C_{it}), which is predominantly determined by the gate dielectric. Without a depletion layer capacitance that is typical for a bulk semiconductor FET, the general relation for *SS* in CNTFETs can be simplified to[8]

$$SS = \frac{kT}{e} ln10 \times \left(1 + \frac{C_{it}}{C_g}\right), \quad (1)$$

where k is Boltzmann's constant, T is the temperature, e is the charge of an electron, and C_g is the geometric gate capacitance ($C_g = \varepsilon_o \varepsilon_r A/t_{ox}$, where ε_o is the permittivity of free space, ε_r is the relative dielectric constant, A is the area of the gate, and t_{ox} is the oxide thickness). Hence, C_{it} plays a crucial role in achieving low *SS* CNTFETs.

Lanthanum oxide has been investigated by several groups as a replacement candidate for SiO_2.[9,10] Much of the interest was motivated by the combination of high dielectric constant ($\varepsilon_r \approx 27$) and thermodynamic stability when placed in contact with Si.[11] Unfortunately, the presence of positive charge was found to induce significant flatband voltage shifts, limiting the usefulness of lanthanum oxide in its pure form for silicon MOSFETs.[9] Lanthanum oxides with excess oxygen have also been reported for low-temperature deposition.[12]

In this work, lanthanum oxide is explored as a gate dielectric for locally bottom gated CNTFETs. Results show that the LaO_x film provides a more favorable interface to the CNT channel, helping to minimize C_{it} and consistently yield devices with low *SS*. All devices in the study were fabricated on high resistivity Si substrates capped with 1 μm SiO_2. Local bottom gates of 20 nm Pd were fabricated using electron-beam lithography (EBL), metal deposition, and lift-off in acetone. The LaO_x films were deposited in a Riber 2300 molecular beam epitaxy/chemical beam epitaxy (MBE/CBE) system. Base pressure prior to deposition was 5×10^{-10} Torr and process pressure was 5×10^{-5} Torr by evaporating La in a high temperature Knudsen cell in a molecular oxygen environment, giving a deposition rate of 2.3 nm/min. The La cell and substrate are surrounded by liquid nitrogen shrouds, holding the substrate temperature during deposition to the range −41 to −38 °C as indicated with a tungsten/rhenium thermocouple spaced approximately 1/16 of an inch behind the rotating substrate. Following the LaO_x formation, CNTs were dispersed

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from solution onto the substrate in the same manner as reported in previous work.[13] There was no special preparation of the LaO_x surface prior to nanotube deposition. Finally, source/drain contacts of Pd were formed using EBL, metal deposition, and lift-off. All devices have a channel length (L_{ch}) of ~80 nm and were electrically tested in air, with no further treatments unless otherwise mentioned.

A schematic of the CNTFET structure is given in Figure 1(a), along with the $I_d - V_{gs}$ curves from a representative device with a 5.7 nm thick LaO_x dielectric in Figure 1(b). Note how close the 63 mV/dec *SS* is to the theoretical limit of 60 mV/dec. Also important is that the *SS* shows only a mild increase at the two decades of I_d immediately preceding the *on*-state; an increase that could be due to small Schottky barriers. As mentioned previously, the ability to show a single CNTFET with an impressive *SS* is not novel in and of itself. In order for a dielectric to be truly useful, it must enable a consistent yield of low *SS* devices, which is suggestive of uniformity in the dielectric quality and in the dielectric-CNT interface.

In order to characterize the thickness and composition of the lanthanum oxide layer, medium energy ion scattering (MEIS) was employed. As illustrated in the schematic of Figure 2(a), MEIS uses a 100 keV beam of protons that backscatter from nuclei in the film via Rutherford scattering. The backscattered protons are detected and provide a linear depth scale by virtue of the energy loss. Two MEIS curves are shown in Figure 2(b) that were used to determine the thickness of the two films—3.5 nm and 5.7 nm. Additionally, the total number of atoms in a film, including oxygen, can be determined by the width of the La peak, while the height of the peak determines the quantity of La atoms. Hence, the MEIS data are used to determine the composition of the films, which are oxygen-rich, with about a 3:1 O:La ratio (LaO_3) as deposited.

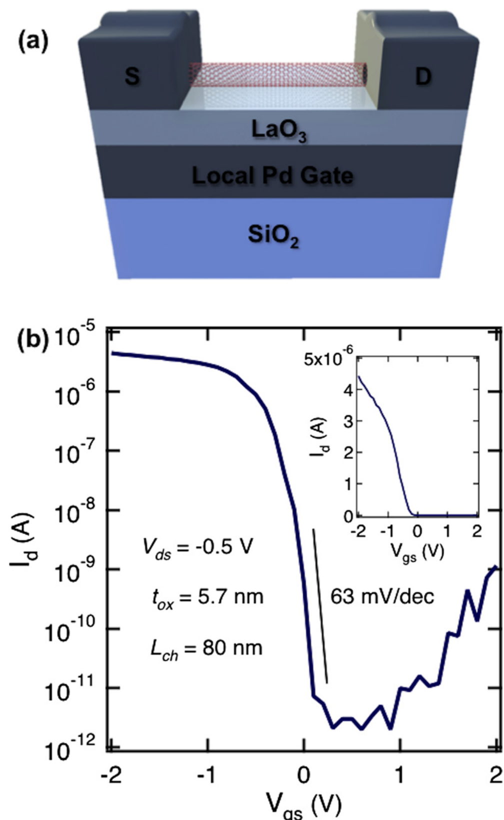

FIG. 1. (a) Schematic of device structure, including 5.7 nm LaO_x gate dielectric, a local Pd gate, and Pd source/drain contacts. Channel length for all devices is 80 nm. (b) Subthreshold curve for a representative device showing superb switching behavior with a subthreshold swing of 63 mV/dec and ON/OFF ratio > 10^6. A transfer curve for the same device is inset.

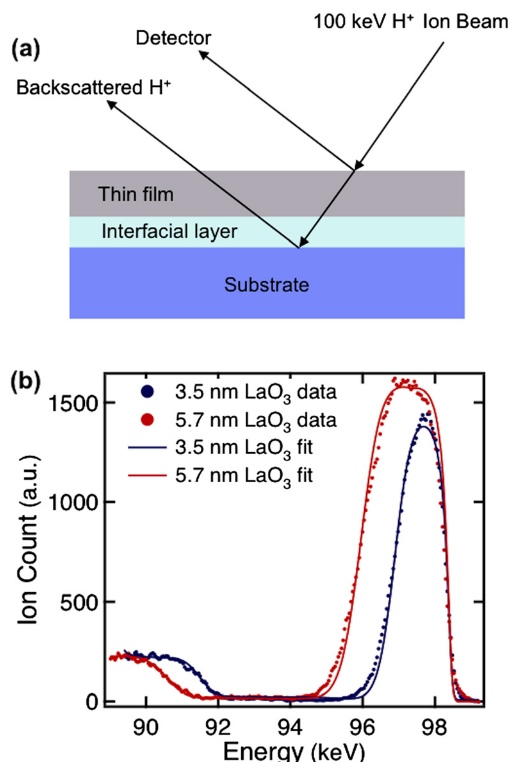

FIG. 2. (a) Schematic illustrating the MEIS film characterization process. (b) MEIS curves from two separate lanthanum oxide films with thicknesses of 3.5 nm and 5.7 nm and composition of LaO_3.

To determine the ability of the LaO_3 to consistently yield low *SS* devices, more than 40 CNTFETs were fabricated using the dielectric with a thickness ranging from 3.5 to 5.7 nm among different substrates. A representative set of subthreshold curves from 14 devices are plotted in Figure 3(a). The average *SS* of 73 mV/dec, as obtained from all CNTFETs tested, is marked with a line in Figure 3(a), and is the lowest *SS* reported to date from a demonstrated set of several dozen nanotube devices. There was an average of 400 mV hysteresis in the devices when V_{gs} was swept from −2 to 2 V at a drain-source bias of $V_{ds} = -0.5$ V. This level of hysteresis is comparable to recent results for CNTFETs on SiO_2, which showed that the hysteresis arises from surface charges that can largely be eliminated from such bottom-gated CNTFETs by applying an appropriate passivation layer.[13]

An important consideration in comparing *SS* is the strong dependence on device structure. Nanotubes have been integrated into a wide range of different device designs, each operating slightly differently. Some devices have large ungated regions between the channel and the contacts as opposed to having the CNT channel connect straight to the contacts, as in the present structure. These underlap regions are typically doped, either chemically or electrostatically using a separate global/substrate gate, thus eliminating the

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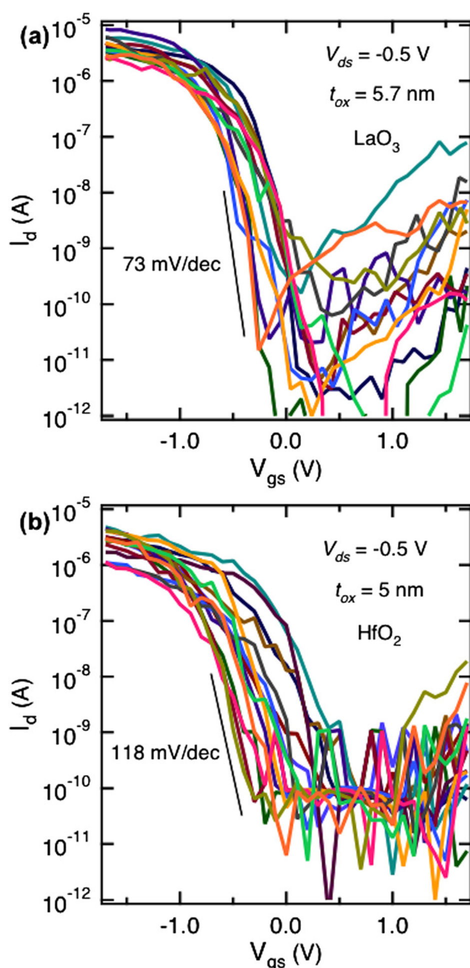

FIG. 3. (a) Subthreshold curves from 14 representative CNTFETs that have LaO_3 as their dielectric. The noted 73 mV/dec is the average *SS* from the total of 42 devices that were tested. (b) Subthreshold curves from 14 representative CNTFETs that have HfO_2 as their dielectric in the same device geometry as the LaO_3 CNTFETs. The average *SS* of 118 mV/dec is marked in the plot, as determined from the total of 64 devices that were tested.

impact of Schottky barrier tunneling on *SS*. Because it is not possible to parse through all of the intricacies among different CNTFET devices, it is most helpful to compare the performance of the LaO_3 to another dielectric integrated in the same geometry. Hence, a set of CNTFETs were fabricated in the same geometry with a CVD-deposited HfO_2 dielectric. Subthreshold curves from 14 representative devices out of the set of 64 are plotted in Figure 3(b). We note that the quality of a dielectric has some dependency on the process used to deposit or grow the film; hence, the results for all dielectrics demonstrated herein could be improved by optimization of the growth process and conditions. The process used for the HfO_2 film is a common CVD growth as used in previous CNTFET work.[1,13,14]

Comparing the subthreshold curves in Figure 3 provides valuable insight into how LaO_3 compares to the more common HfO_2. First, it is clear that the *SS* is substantially lower in the LaO_3 devices—the average is nearly 40% smaller than for the HfO_2. Assuming no Schottky barrier impact on *SS*, Eq. (1) would suggest that the C_{it} for the HfO_2 devices is five times greater than for the LaO_3. Also, the range of threshold voltages (V_{th}) is less than half for LaO_3, at 0.41 V versus 0.88 V for HfO_2; the V_{th} variation in CNTFETs was recently shown to be determined primarily by interface charges between a CNT and the supporting dielectric.[13] This tighter V_{th} distribution is evidence of LaO_3 providing a better interface to CNTs than HfO_2. Finally, comparing the curves in Figure 3 shows that the HfO_2 devices are much noisier, particularly in the *on*-state. The lower level of noise in I_d is another indication that the LaO_3-CNT interface contains less traps and/or stray charge that can contribute to such noise in CNTFETs.[15]

As mentioned above, the geometry of a CNTFET plays a considerable role in the switching behavior, making comparisons of devices in the same geometry much more meaningful. However, considering a number of studies from different dielectrics can be insightful in terms of the range of *SS* that is obtained for each dielectric. Such a comparison is made in Figure 4, where studies that used SiO_2,[7,13,15–18] Al_2O_3,[16,19,20] and HfO_2 (Refs. 1, 14, and 21–23) are all compared to the LaO_3 results from this work. The Figure 4 plot makes clear how much smaller the range of *SS* is from the present devices compared to the most common CNTFET gate dielectrics. Note that the dielectric constant for the different materials may not have been reported in the studies and is therefore an approximation.

In conclusion, we have explored the use of lanthanum oxide (LaO_3) as a gate dielectric for CNTFETs. Devices with subthreshold swings down to 63 mV/dec at room temperature were realized, with an average among 42 devices of 73 mV/dec—HfO_2 was employed in the same geometry and yielded an average of 118 mV/dec with higher noise and a larger range in threshold voltage. MEIS was used to characterize the thickness and composition of the LaO_3 films. Finally, the *SS* was compared to studies that used one of the three most common dielectrics for CNTFETs, highlighting how much better and more consistent the switching behavior is for the LaO_3 CNTFETs. Overall, these results indicate the importance of dielectric-CNT interface quality for obtaining more consistent device performance.

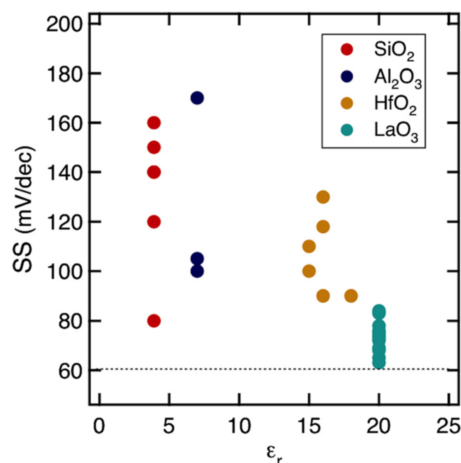

FIG. 4. Subthreshold swing versus the approximate dielectric constant from papers involving the three most common gate dielectrics used with CNTFETs. This shows that nearly the entire range of *SS* from the LaO_3 devices falls below the best previously reported *SS* from one of the common dielectrics.

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