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Sustained Sub-60 mV/decade Switching via the Negative Capacitance Effect in MoS_2 Transistors

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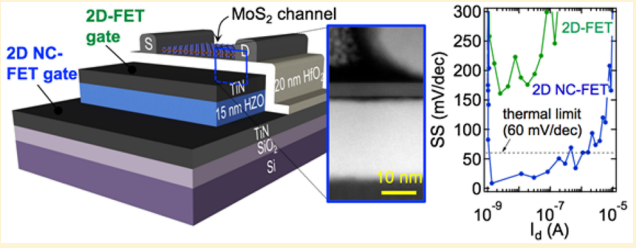
Supporting Information

ABSTRACT: It has been shown that a ferroelectric material integrated into the gate stack of a transistor can create an effective negative capacitance (NC) that allows the device to overcome "Boltzmann tyranny". While this switching below the thermal limit has been observed with Si-based NC field-effect transistors (NC-FETs), the adaptation to 2D materials would enable a device that is scalable in operating voltage as well as size. In this work, we demonstrate sustained sub-60 mV/dec switching, with a minimum subthreshold swing (SS) of 6.07 mV/dec (average of 8.03 mV/dec over 4 orders of magnitude in drain current), by incorporating hafnium zirconium oxide ($HfZrO_2$ or HZO) ferroelectric into the gate stack of a MoS_2 2D-FET. By first fabricating and characterizing metal−ferroelectric−metal capacitors, the MoS_2 is able to be transferred directly on top and characterized with both a standard and a negative capacitance gate stack. The 2D NC-FET exhibited marked enhancement in low-voltage switching behavior compared to the 2D-FET on the same MoS_2 channel, reducing the SS by 2 orders of magnitude. A maximum internal voltage gain of ~28× was realized with ~12 nm thick HZO. Several unique dependencies were observed, including threshold voltage (V_{th}) shifts in the 2D NC-FET (compared to the 2D-FET) that correlate with source/drain overlap capacitance and changes in HZO (ferroelectric) and HfO_2 (dielectric) thicknesses. Remarkable sub-60 mV/dec switching was obtained from 2D NC-FETs of various sizes and gate stack thicknesses, demonstrating great potential for enabling size- and voltage-scalable transistors.



KEYWORDS: *Negative capacitance, ferroelectric, MoS_2, 2D, field-effect transistor, steep switching, $HfZrO_2$, HZO*

Metal−oxide−semiconductor field-effect transistor (MOSFET) scaling has been impeded over the past decade by the inability to scale the operating voltage (V_{DD}), resulting in excess heat generated during switching.[1−3] Essential to scaling V_{DD} is the subthreshold swing (SS), a metric of how effectively the applied gate voltage (V_{gs}) can modulate the drain current (I_d) by 1 order of magnitude, or one decade (dec). The SS is thermally limited to 60 mV/dec at room temperature with normal dielectric materials because of the nonscalable Boltzmann factor (kT/q), where k is the Boltzmann constant, T is the temperature, and q is the elementary electronic charge. In 2008, it was theorized that, if a ferroelectric material were incorporated into the transistor gate stack, it would create an effective negative capacitance where the insulator capacitance (C_{ins}) becomes negative while the substrate capacitance (C_s) remains positive and the body factor, ($1 + C_s/C_{ins}$) reduces below 1.[4]

$$SS = \frac{\partial V_{gs}}{\partial(\log_{10} I_d)} = \frac{\partial V_{gs}}{\partial \psi_s}\frac{\partial \psi_s}{\partial(\log_{10} I_d)} = \left(1 + \frac{C_s}{C_{ins}}\right) \times \left(\frac{kT}{q}\ln 10\right) \quad (1)$$

This would amplify the modulation of the surface potential in the channel (ψ_s) over V_{gs} and allow the SS to fall below 60 mV/dec, giving rise to steep switching and, potentially, low-voltage operation.

The incorporation of ferroelectrics into FETs to harness the NC effect and overcome "Boltzmann tyranny" has shown tremendous progress.[5] To date, sub-60 mV/dec switching has been observed mainly with silicon-based MOSFETs (NC-

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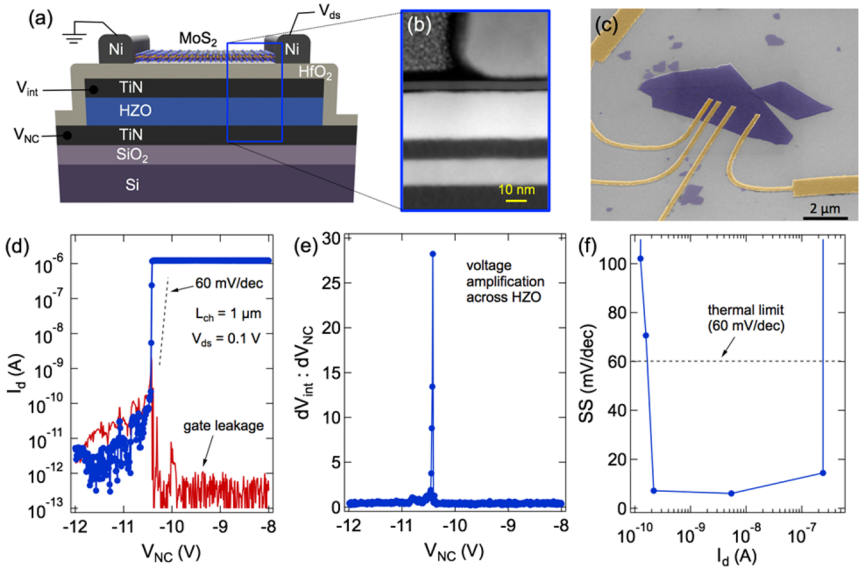

Figure 1. 2D negative capacitance FET with sub-60 mV/dec switching. (a) 2D NC-FET device schematic illustrating characterization configuration. (b) STEM image showing the layers and thicknesses of the gate stack, the individual MoS_2 layers, and a portion of the Ni electrode. (c) False-colored, tilted SEM image of MoS_2 channel and contacts (20 nm Ni) over MFM-oxide gate stack. (d) Subthreshold curve of 2D NC-FET plotted with gate leakage current. (e) Dramatic increase in V_{int} with respect to the applied V_{NC} occurring in the region of sub-60 mV/dec switching as is characteristic of the NC effect. (f) Point-by-point subthreshold swing (SS) vs drain current showing the sub-60 mV/dec switching extending over more than four decades.

FETs) using ferroelectrics ranging from lead zirconium titanate (PZT) to CMOS-compatible, doped-HfO_2.[6−18] These devices have achieved internal voltage gains greater than 6× the applied V_{gs}, allowing for sub-60 mV/dec switching at room temperature.[7,19−22] The realization of this enhanced switching behavior is achieved by simply incorporating an additional layer of ferroelectric material into the gate stack of existing, state-of-the-art MOSFETs.[15,16]

Some of the most encouraging recent progress in Si-based NC-FETs has been a result of the CMOS-compatible HZO ferroelectric. Doped hafnium oxide thin films are simple, binary oxides with a nonperovskite crystal structure and relatively low permittivities that can be grown using atomic layer deposition (ALD) processes.[23−26] Ferroelectricity has been demonstrated in yttrium-, silicon-, and zirconium-doped hafnium oxides.[24,27,28] Zr-doped HfO_2 films are favored for integration into CMOS technology for chemical and physical similarities to HfO_2 and low crystallization temperatures. With top and bottom titanium nitride (TiN) electrodes, Zr-doped HfO_2 films have been found to exhibit the largest remnant polarizations when in a 1:1 Hf:Zr ratio, $HfZrO_2$, or HZO.[29] Moreover, HZO exhibits an inverse scaling behavior of polarization versus thickness compared to other prominent ferroelectrics; for HZO, polarization is enhanced as the thickness is scaled down.[23,24]

While the progress made toward low-voltage, NC-FETs is very encouraging, the Si-based channels are rapidly approaching physical scaling limits.[23] Maintaining electrostatic control becomes uncertain, regardless of the gating effect, especially as technology approaches the 5 nm node within the next 5−10 years. Replacing the Si channel with a two-dimensional (2D) material, such as a 2D transition metal dichalcogenide (TMD), is one path that has shown promise for overcoming the issues that plague the conventional dimensional scaling of transistors. 2D TMDs have been studied as channel materials in 2D-FETs for the numerous benefits they provide, with the most promising being their atomic thinness that enables aggressive scaling via enhanced electrostatic control of the channel.[3,30−36] Replacing the 3D Si-channel with a 2D material can also improve the stability of C_s, as 2D materials offer increased surface area to volume ratio, creating a more pronounced NC-effect.[37,38] There is one recent report of integrating a ferroelectric in the gate stack of a 2D MoS_2 FET to create a 2D NC-FET, which did in fact yield sub-60 mV/dec switching. However, the demonstrated device used an unstable polymeric ferroelectric that led to rapid degradation of the device and the inability to fully characterize its behavior, including such critical aspects as hysteresis.[39] Replacing the ferroelectric polymer with a more technologically relevant, reliable ferroelectric, like doped-hafnium oxides, is needed to study the true performance and operation of such 2D NC-FETs.

In this work, 2D NC-FETs are demonstrated that combine 2D MoS_2 channels with HZO ferroelectrics to yield stable and reproducible sub-60 mV/dec switching over multiple decades of current. The stability of C_s enables an internal voltage gain of the applied V_{gs} by 28×, allowing the abrupt transition between on- and off-states at SS as low as ∼6 mV/dec. The reliability of the NC-effect is demonstrated across devices of multiple channel lengths (L_{ch}) and different MoS_2 flakes. An interesting dependence of the 2D NC-FET hysteresis and subthreshold swing on drain−source bias is observed. Also, the relationship between HZO thickness and resultant threshold voltage is revealed, showing encouraging capability to realize 2D NC-FETs that can fully operate at low voltage. Additionally, we compare the performance of a 2D-FET to that of a 2D NC-FET from the same MoS_2 channel, showing an improvement in the SS of 2 orders of magnitude.

To most fully realize ferroelectricity in HZO films, appropriate capping layers must be used with an annealing step to drive formation of the orthorhombic crystal phase.[23] To fabricate the 2D NC-FETs, TiN metallic electrodes were used to sandwich the HZO, with the topmost TiN layer (between

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the HZO and HfO_2 layers in Figure 1a) serving as the internal gate electrode (V_{int}). Details of the fabrication process are included in Figure S1, where the metal-ferroelectric-metal (MFM) capacitors are first fabricated using atomic layer deposition (ALD). After characterization of the MFM capacitors to ensure ferroelectric behavior (see Figure S2), a HfO_2 gate dielectric layer was grown over the MFM capacitors via ALD. 2D flakes of MoS_2 were mechanically exfoliated over the HfO_2-coated MFM capacitors, with thickness confirmation from atomic force microscopy (AFM). Contacts, leads, and source/drain pads were established with electron beam lithography (EBL). Thicknesses for each layer were extracted from cross-sectional scanning transmission electron microscopy (STEM) imaging, as shown in Figure 1b.

The V_{int} electrode (top TiN layer in the MFM stack) was previously shown to be crucial for mitigating interfacial effects that can arise between the ferroelectric and the gate oxide.[39] The inclusion of this layer in the present device structures also allowed for characterization of the same MoS_2 channel as a traditional, bottom-gated 2D-FET for comparison to a 2D NC-FET. Additionally, the V_{int} layer allowed for monitoring of the internal voltage gain (change in V_{int} versus change in applied V_{gs}) during the operation of the 2D NC-FET. The ferroelectric performance of the TiN−HZO−TiN MFM capacitors used in this study is shown in their polarization versus electric field (P−E) properties found in Figure S2. The general layout of the devices is given in the scanning electron microscopy (SEM) image in Figure 1c, where multiple L_{ch} were included on the same MoS_2 flake.

The subthreshold characteristics of a 2D NC-FET with an MoS_2 thickness of ∼5 nm [having 12.3 nm HZO, 22.8 nm HfO_2, 1 μm channel length (L_{ch}), and drain−source bias (V_{ds}) of 0.1 V] are given in Figure 1d−f. Here, V_{NC} is the gate, V_S is the grounded source, and V_{int} is a floating gate that allowed the voltage at the V_{int} electrode to be measured. The SS falls below the thermal limit for over 4 decades of current, with a minimum of 6.07 mV/dec and average of 8.03 mV/dec. Along with the drop in I_d at about the threshold voltage (V_{th}), there is a simultaneous spike in the leakage current (I_g) that is attributed to the amplified gate field across the oxide. In fact, this amplification is seen through the change in the voltage on V_{int} with respect to the change in applied gate voltage (V_{NC}), which increases ∼28× in the region of sub-60 mV/dec switching, as shown in Figure 1e. The gain observed at V_{int} with the 2D NC-FET is a dramatic increase over that observed from 3D NC-FETs, which generally demonstrate a maximum improvement of less than 7×.[4,6,7] This is partially attributed to the more stable C_s from the 2D MoS_2 that enables the realization of the NC effect.

The abrupt and dramatic switching behavior displayed in Figure 1d is a direct effect of integrating a ferroelectric layer into the gate stack. This is explained mathematically through the Landau−Khalatnikov (L−K) equation, which relates the polarization to the applied field, the voltage across the ferroelectric (V_{Fe}), and the ferroelectric thickness (t_{Fe}):

$$E = 2aP + 4bP^3 + 6cP^5 = \frac{V_{Fe}}{t_{Fe}} \quad (2)$$

The α parameter is material- and temperature-dependent, while β and γ are strictly material-dependent parameters. For ferroelectric operation, α has a negative value, while β can be either positive or negative. γ is considered to be always positive. Simulations using the L−K equation show a brief region where the voltage across the ferroelectric is of opposite polarity to that of the applied voltage, indicating the negative capacitance effect that produces steep switching.[4,6] This also explains the observed voltage amplification behavior. With the ferroelectric in series with the 2D-FET (shown in Figure 2), the change in

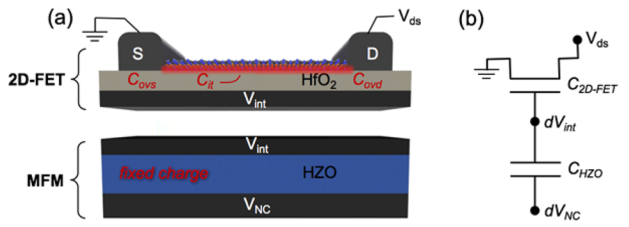

Figure 2. Voltage and capacitor network in 2D NC-FET. (a) Device schematic split into the metal−ferroelectric−metal (MFM) capacitor and the 2D-FET. Indicated in red are some of the sources of parasitic behavior in the device, including overlap capacitance between the source/drain and V_{int} (C_{ovs} and C_{ovd}), fixed charges, and interface traps (with associated C_{it}). (b) Diagram of the 2D NC-FET gate stack showing the primary voltages and capacitances. Note that the $C_{2D\text{-}FET}$ includes the capacitance from the HfO_2 gate dielectric as well as the capacitance from the MoS_2 channel (C_s).

the applied voltage (V_{NC}) can be written as the sum of the differential voltages between the ferroelectric material (dV_{Fe}) and the 2D-FET (dV_{int}):

$$dV_{NC} = dV_{Fe} + dV_{int} \quad (3)$$

Thus, a change in dV_{Fe} opposite in polarity to that of the applied V_{NC} causes the differential potential felt at the 2D channel (dV_{int}) to be larger than V_{NC}.

Further characterization of these 2D NC-FETs revealed some interesting dependencies on V_{ds}, as seen in Figure 3. All V_{ds} conditions achieved sub-60 mV/dec switching; however, a larger applied V_{ds} produced a lower minimum SS and a larger range over which steep switching occurred. A similar observation was made for the hysteresis − as V_{ds} increased, hysteresis decreased until negligible. The effect of V_{ds} on hysteresis can be explained as a drain-side switching phenomenon, where a reduction in V_{NC} causes the gate-to-drain voltage (V_{gd}) to rise. The overlap in the device structure (source and drain contacts are overlapping the gate stack as shown in Figure 1a) prompts the largest field to drop at the drain. At some V_{gd}, the ferroelectric switching depletes the region under the drain, creating an abrupt decrease in I_d. With larger V_{ds}, the depletion occurs much closer to V_{th}, lowering the hysteresis. This drain-side switching effect can be mitigated by employing a self-aligned gate, which minimizes the overlap between the gate and drain to reduce the impact of the drain on channel switching.

An additional aspect of the hysteretic behavior in these devices is that the sub-60 mV/dec switching occurs exclusively on the negative sweep, whereas the positive sweep exhibits a more traditional subthreshold response. This asymmetry in the curves based on sweep direction results from the presence of charge traps in the gate stack heterostructure, which minimize polarization effects by screening the electric field. After the traps have been neutralized, the ferroelectric becomes polarized, resulting in the abrupt jump that is able to be observed in the reverse sweep. However, for the positive sweep,

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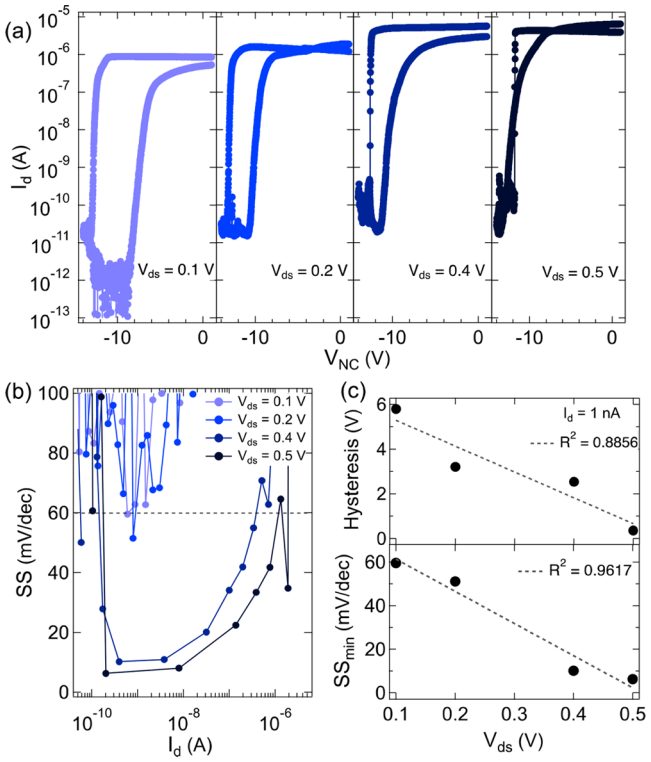

Figure 3. Drain bias-dependent behaviors of hysteresis and SS in 2D NC-FETs. (a) Hysteretic subthreshold curves of a 2D NC-FET at increasing V_{ds} (L_{ch} = 1 μm). (b) Point-by-point subthreshold swing vs drain current showing decreasing SS with increasing V_{ds}. (c) Top: decrease in hysteresis with increasing V_{ds}. The hysteresis was measured at $I_d = 10^{-9}$ A. Bottom: minimum SS dependence on V_{ds}.

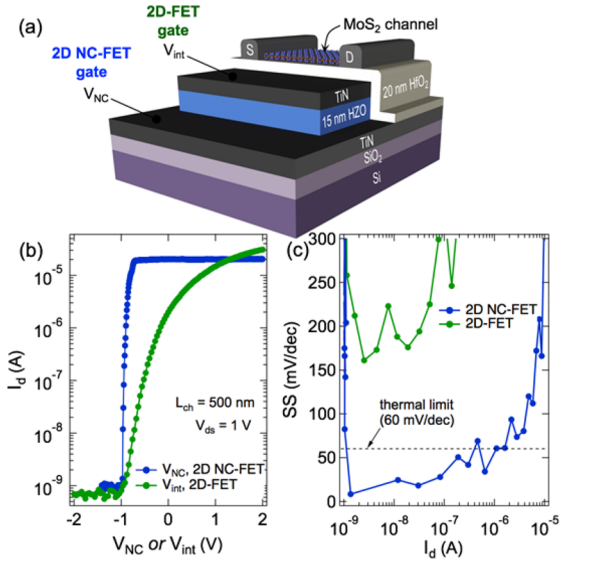

Figure 4. Comparison of 2D NC-FET with 2D-FET on same MoS_2 channel. (a) Cross-sectional schematic of the device illustrating V_{int} and V_{NC} terminals. (b) Subthreshold curves from the same MoS_2 channel gated either as a 2D-FET (using V_{int} as the active gate) or as a 2D NC-FET (using V_{NC}). Note the threshold voltage of the 2D NC-FET was shifted positive to match up with that of the 2D-FET for a more useful comparison (see Figure S5). (c) Subthreshold swing from the 2D-FET and 2D NC-FET. The 2D-FET operates well above the thermal limit, while the 2D NC-FET has a large range in drain current where the SS is below 60 mV/dec.

any such rapid polarization is stifled by the emptying/charging of traps that leads to a more gradual switching behavior.

The subthreshold performance of a MoS_2 2D-FET with ~8 nm MoS_2 is compared to that of the respective 2D NC-FET (on the same MoS_2 channel) in Figure 4. Note that characterization of the 2D-FET was accomplished by using V_{int} as the gate electrode. Comparison of the same 500 nm channel transistor at V_{ds} = 1 V demonstrates the more advantageous switching behavior of the 2D NC-FET. A dramatic improvement of almost 2 orders of magnitude is seen in the SS of the 2D NC-FET (minimum SS = 8.5 mV/dec) when compared to that of the 2D-FET (minimum SS = 161 mV/dec). Direct comparison of these devices shows the improvement in subthreshold characteristics produced from the NC-effect, and it indicates that any detrimental interfacial effects were minimized. In all, Figure 4 suggests improvement in subthreshold characteristics is strictly due to the addition of the ferroelectric layer and the realization of the NC effect.

The HZO thickness of the device in Figure 4 was increased from 12.3 to 18.6 nm to avoid any unfavorable effects from nonuniform HZO deposition across the wafer. The HfO_2 thickness was also increased from ~22.8 to ~45.7 nm, to ensure complete coverage of the MFM stack. Note that these film thicknesses were verified by extraction from cross-sectional STEM images, such as the one shown in Figure 1b. Also, note that the subthreshold curve of the 2D NC-FET has been shifted by ~26 V to provide a more useful comparison between the 2D NC-FET and 2D-FET that are using the same MoS_2 channel.

The large negative shift in threshold voltage for the 2D NC-FET compared to the 2D-FET stems from a combination of factors, including the capacitance from the overlapping source/drain contacts with the gate (illustrated in Figure 2) and trapped charges in the HZO and HfO_2 layers. First, to determine the impact of the overlap capacitance on the threshold voltage shift, a model was developed for the 2D NC-FET, as described in the Supporting Information section. Results of the model, shown in Figure S3, give evidence that an increase in the overlap capacitance (C_{ov}) results in a more negative threshold voltage shift. There was a limitation on the amount of C_{ov} that could be introduced in the model, and a C_{ov} between 20% to 90% of the 2D-FET capacitance ($C_{2D\text{-}FET}$) was investigated. The actual C_{ov} in our experimental 2D NC-FETs is even larger than 90% of $C_{2D\text{-}FET}$ since the entire source and drain contact pads overlap with V_{int}. However, C_{ov} is still not solely responsible for the observed negative shift in threshold voltage, as the presence of trapped charges within the HZO and/or the HfO_2 layers was also identified as a contributing factor. This was confirmed by comparing 2D NC-FETs fabricated with different thicknesses of the HZO and HfO_2 (both layers were scaled concurrently). When the HZO was increased in thickness by ~50% and HfO_2 by ~100%, the negative shift in threshold voltage more than doubled. Since the relative C_{ov} compared to $C_{2D\text{-}FET}$ would be nominally consistent for these devices, this result gives evidence for the substantial impact that the HZO and HfO_2 thicknesses play in the observed threshold shift. As thinning the HZO will bring V_{th} closer to 0 V, the recent demonstrations of sub-2 nm HZO exhibiting ferroelectricity is very encouraging for future iterations of these devices.[29]

Additional fabricated devices point to the reliability and repeatability of the NC effect in 2D NC-FETs. The subthreshold characteristics of 2D NC-FETs using another MoS_2 flake ~7 nm thick are given in Figure S4a. Here, the

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ferroelectric and HfO_2 thicknesses were 12.3 and 22.8 nm, respectively, and L_{ch} = 500 nm. Providing for variations across different MoS_2 flakes, this device displays comparative performance to that shown in Figure 2a, where a sub-60 mV/dec SS is achieved at each V_{ds}. The observed voltage gains (dV_{int}/dV_{NC}) again occur at V_{th}, as seen in Figure S4c. Decreases observed in the gain compared to the device in Figure 1e are attributed to current leakage along the grain boundaries of the thicker ferroelectric in the MFM capacitor. This type of leakage produces "leaky" ferroelectric behavior, where the edges of the $P-E$ characteristics are slightly rounded, as shown from the 600 °C anneal characteristic in Figure S2c. Regardless of the drop, the voltage gain at each V_{ds} is still comparable to, if not greater than, that of reported NC-FETs from 3D silicon channels.[7,19−22]

The effects of varying the sweep rate on the subthreshold characteristics were also investigated. These devices utilized the thicker HZO and HfO_2 films of 18.6 and 45.7 nm, respectively. Hysteresis curves at measurement lengths of 6, 8, and 10 μs corresponding to sweep rates of 19.84, 16.88, and 11.90 Hz, respectively, are provided in Figure S6a. The data was obtained from the same 2D NC-FET, with all other device parameters held constant. Of most importance are the linear shifts observed in the threshold voltages and in the hysteresis in Figure S6b. Shorter measurement times (higher sweep rates) lowered the hysteresis present in the device, yet had no effect on either I_{OFF} or on the return sweep V_{th}. While this effect requires further investigation to interpret its precise/quantitative origin, it is attributed to interface traps in the gate stack, especially since the sweep rate dependence of hysteresis in a traditional MFM is typically opposite the observation in these devices (hysteresis for MFMs increases with sweep rate). In this case, the small changes in sweep rate explored in Figure S6 are modulating the impact of interface traps based on the trap charging rates—a longer voltage pulse duration (slower sweep rate) allows for more traps to charge and thus yields more hysteresis. This has been observed in other nanomaterial-based FETs, where small decreases in the sweep rate yielded significant increases in hysteresis.[40] As nanomaterials offer no surface bonding to their supportive oxide substrate, they tend to be more prone to deleterious interface trap effects such as these. A more optimal 2D NC-FET device will be one that has minimized the interface trap density so as to minimize its impact on operation in these ways.

In conclusion, 2D NC-FETs with repeatable, sustained sub-60 mV/dec switching have been demonstrated using 2D MoS_2 channels and CMOS-compatible HZO ferroelectric. The 2D MoS_2 provides the most scalable channel to stabilize the NC-effect and achieve large voltage gains, resulting in SS below the thermal limit over more than 4 orders of magnitude of drain current. Extensive improvement in subthreshold performance was shown with the 2D NC-FET compared to a 2D-FET on the same MoS_2 channel. Shifts in V_{th} were found to be correlated with overlap capacitance and HZO and HfO_2 thickness—the thinner the HZO and HfO_2 layers, the lower (closer to 0 V) the V_{th}. Analysis of hysteresis, including its dependence on bias and sweep rate, and of the voltage gain were also included. These results show great promise for 2D NC-FETs to enable scalable, low-voltage transistors.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.7b01584.

2D NC-FET fabrication and characterization processes, modeling of 2D NC-FET, voltage gain with increasing V_{ds} and repeatability, threshold voltage shift, sweep rate dependence, and energy-dispersive spectroscopy (PDF)

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Author Contributions

F.A.M. and A.D.F. designed all experiments. F.A.M. completed all fabrication and characterization with the assistance of Y.C.L. in ferroelectric characterization and K.P. in ALD processing. G.B.R. helped develop and qualify ALD processes. S.K. and S.S. performed device simulations. F.A.M., S.S., S.K., and A.D.F. analyzed and interpreted all data. All authors commented on the manuscript.

Notes

The authors declare no competing financial interest.

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