APPLIED PHYSICS LETTERS 109, 093101 (2016)

Sub-60 mV/decade switching in 2D negative capacitance field-effect transistors with integrated ferroelectric polymer

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(Received 18 May 2016; accepted 1 August 2016; published online 29 August 2016)

There is a rising interest in employing the negative capacitance (NC) effect to achieve sub-60 mV/decade (below the thermal limit) switching in field-effect transistors (FETs). The NC effect, which is an effectual amplification of the applied gate potential, is realized by incorporating a ferroelectric material in series with a dielectric in the gate stack of a FET. One of the leading challenges to such NC-FETs is the variable substrate capacitance exhibited in 3D semiconductor channels (bulk, Fin, or nanowire) that minimizes the extent of sub-60 mV/decade switching. In this work, we demonstrate 2D NC-FETs that combine the NC effect with 2D MoS_2 channels to extend the steep switching behavior. Using the ferroelectric polymer, poly(vinylidene difluoride-trifluoroethylene) (P(VDF-TrFE)), these 2D NC-FETs are fabricated by modification of top-gated 2D FETs through the integrated addition of P(VDF-TrFE) into the gate stack. The impact of including an interfacial metal between the ferroelectric and dielectric is studied and shown to be critical. These 2D NC-FETs exhibit a decrease in subthreshold swing from 113 mV/decade down to 11.7 mV/decade at room temperature with sub-60 mV/decade switching occurring over more than 4 decades of current. The P(VDF-TrFE) proves to be an unstable option for a device technology, yet the superb switching behavior observed herein opens the way for further exploration of nanomaterials for extremely low-voltage NC-FETs. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4961108]

Until recently, ferroelectric materials were utilized almost exclusively for memory devices, as they exhibit large hysteresis from remnant polarizations that allow for reproducible "read" and "write" operations.[1–3] In 2008, another property of ferroelectric materials sparked a great deal of interest, when it was theorized that a ferroelectric incorporated into the gate stack of a field-effect transistor (FET) would act as a "step-up amplifier" by expressing an effective negative capacitance (NC).[4] This NC effect would lower the subthreshold swing (SS) of the FET below the thermal limit of 60 mV/decade (60 mV of applied gate potential V_{gs} to modulate the drain current I_d by one order of magnitude or decade) by decreasing the value of the body factor (m) below one

$$SS = \frac{\partial V_{gs}}{\partial(\log I_d)} = \frac{\partial V_{gs}}{\partial \psi_s}\frac{\partial \psi_s}{\partial(\log I_d)} = \left(1+\frac{C_s}{C_{ins}}\right)\left(\ln 10\frac{kT}{q}\right), \tag{1}$$

$$m = \left(1+\frac{C_s}{C_{ins}}\right), \tag{2}$$

where V_{gs} is the gate voltage, I_d is the drain current, ψ_s is the surface potential in the channel, C_s is the substrate capacitance, C_{ins} is the insulator capacitance, k is the Boltzmann constant, T is temperature, and e is the charge of an electron. Prior to the NC effect discovery, it was assumed the body factor of a FET would have a minimum value of one as both the substrate and insulator capacitances would have positive values.

With the continued scaling of transistor technology, the need for a low-voltage device has become paramount. Hence, a surge of research activity is underway that focuses on harnessing the NC effect to reduce the operating voltage in FETs. To date, the NC effect has been studied with ferroelectric materials integrated into silicon-based FETs,[5–14] in which one of the key challenges is the variable substrate/channel capacitance that leads to a diminished sub-60 mV/dec region in the device subthreshold behavior.[5] From Eq. (1), it should be noted that the body factor is dependent on both the insulator capacitance (C_{ins}) and the substrate capacitance (C_s). Destabilizing the substrate capacitance leads to an unstable negative capacitance, making it difficult to realize the full benefits of a NC-FET using a 3D channel material. One solution is to replace the silicon with a 2D, "atomically thin" material offering a more stable capacitance with a reasonable band gap, such as a transition metal dichalcogenide (TMD). The use of TMDs in 2D FETs has rapidly expanded in recent years, with the field growing significantly each day.[15–19] The benefits of using TMDs as the channel material are numerous, one of the most promising of which is their ability to enable aggressively scaled transistors.[20–22] Unfortunately, even with the scaled FETs, there is no clear path for these materials to yield low-voltage switching in a FET without help, such as incorporating a ferroelectric to yield NC within a 2D FET. While there has been some work on combining 2D materials with ferroelectrics for memory devices (i.e., ferroelectric FET or Fe-FET) making use of substantial hysteresis,[23–27] there has yet to be a study on achieving steep subthreshold switching behavior when combining 2D materials and ferroelectrics with an additional gate dielectric layer.

In this work, we report on the fabrication and demonstration of 2D NC-FETs, utilizing molybdenum disulfide

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(MoS_2) as the channel material and ferroelectric copolymer poly(vinylidene difluoride-trifluoroethylene), P(VDF-TrFE), in a 70:30 ratio. P(VDF-TrFE) is a solution-processed ferroelectric polymer that displays ferroelectric behavior at a variety of concentrations and ratios.[3,11,28–34] The P(VDF-TrFE) is integrated into the gate stack of top-gated MoS_2 2D FETs in two configurations: (1) with an interfacial metal layer separating the P(VDF-TrFE) and gate dielectric and (2) without such an interfacial layer. It is observed that the inclusion of the interfacial metal layer enables realization of sub-60 mV/dec switching over several orders of magnitude in drain current. While this NC effect was strongly exhibited in initial device testing, rapid deterioration occurred, suggesting that the use of a polymeric ferroelectric (while helpful for device demonstration) is not favorable for stable operation in scaled FETs. Despite this observed deterioration, the demonstrated 2D NC-FETs with sub-60 mV/dec switching over several orders of magnitude in this work do show great promise for combining the advantages of 2D channel materials with NC-FETs.

Capacitors were initially fabricated to study the response of the P(VDF-TrFE) ferroelectric. Bottom pads were written using electron beam lithography (EBL) and metallized with 5 nm Ti/30 nm Au. A 3% (w/w) P(VDF-TrFE) in methyl ethyl ketone (MEK) was spin-coated over the gold pads and baked, after which a shadow mask was employed to establish the top contact and complete the parallel plate structure. Using this setup, ferroelectric behavior was observed with the 3% solution, seen in Fig. 1(a), though the voltage at which this behavior was present is significantly larger than the typical operating voltage of a 2D-FET. To lower the voltage, the 3% solution was replaced with a 1% P(VDF-TrFE) solution in all further reported results, providing a slight reduction in the voltage required for device operation.

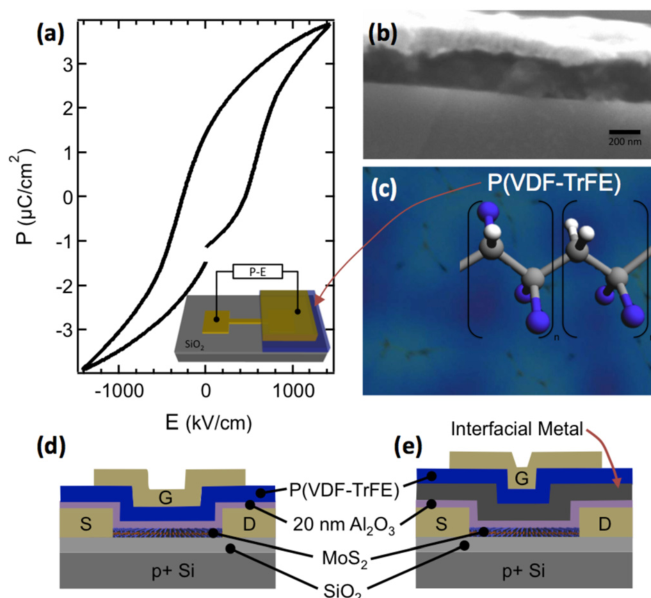

FIG. 1. (a) Polarization vs. electric field curve for a 3% (w/w) P(VDF-TrFE) capacitor with the inset showing schematic of the capacitor structure. (b) SEM cross-sectional view of 1% P(VDF-TrFE) on 10 nm SiO_2 coated with 10 nm Ti/100 nm Au. (c) Optical image of P(VDF-TrFE) showing the inconsistency of the polymer thickness, with molecular structure inset. Schematic cross-sections of the 2D NC-FET structures studied herein (d) without and (e) with an interfacial metal layer between the P(VDF-TrFE) and Al_2O_3 gate dielectric.

The first step in fabricating the 2D NC-FETs was to realize substrate-gated 2D FETs with MoS_2 channels on 10 nm SiO_2, heavily p-doped Si. Having the substrate gate allowed a baseline characterization of the bottom-gated 2D FET after which the same device undergoes further processing to establish the top gate stack. To form the top gate, 20 nm Al_2O_3 was grown via atomic layer deposition (ALD) at 120 °C with precursors trimethyl aluminum (TMA) and water (H_2O). The first device structure considered was the 2D NC-FET without the interfacial metal layer (Fig. 1(d)), so the next step was the deposition of P(VDF-TrFE). The 1% P(VDF-TrFE) solution was spin-coated over the substrate and baked at 140 °C for 600 s. A final top gate to complete the 2D NC-FET was then established using a shadow mask, the results of which are explained in Fig. 2.

With the P(VDF-TrFE) integrated directly on top of the Al_2O_3 gate dielectric, there are interfacial effects that must be considered in the performance of the resulting FET. As shown in Fig. 2(a), an improvement in the subthreshold swing by approximately 50% is obtained with a corresponding drop of the current by an order of magnitude compared to the same device operated with the substrate gate. Despite the reduction in SS, it is still well above the thermal limit of 60 mV/dec at 252 mV/dec, and thus not realizing the full amplification benefit that should be possible in a properly operating NC-FET. This poor performance is attributed to interfacial effects between the polymer and the dielectric, as the presence of ferroelectric behavior in P(VDF-TrFE) is highly sensitive to this interface.[34,35] Despite the deleterious impact of this interface, the 50% reduction in SS is still considered an effect of the ferroelectric polymer. This is because the 10 nm SiO_2 presents a more favorable gate electrostatically compared to the 20 nm Al_2O_3 + 200 nm P(VDF-TrFE), which can be explained by looking at the equivalent oxide

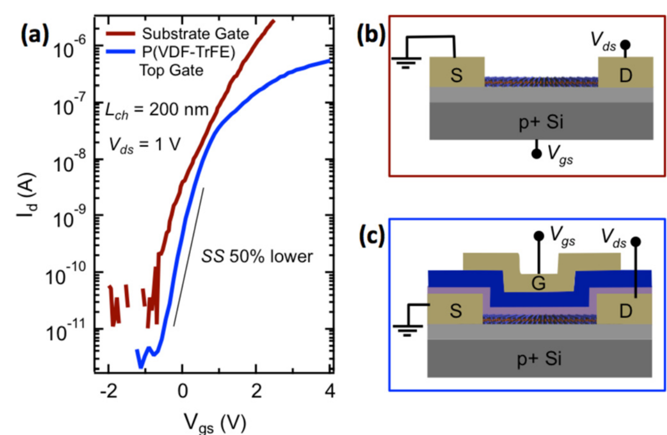

FIG. 2. (a) Comparative subthreshold curves from the same MoS_2 channel that is gated with either the substrate as a 2D FET or the top gate as 2D NC-FET having no interfacial layer between the P(VDF-TrFE) and Al_2O_3 dielectric. Schematics of the (b) substrate-gated and (c) top-gated configurations illustrating the characterization setup. Here, incorporating the ferroelectric polymer into the gate stack resulted in a 50% reduction in SS compared to the substrate-gated 2D FET of the same MoS_2 channel. Note that the threshold voltage of the top-gated 2D NC-FET was shifted by +4.6 V in order to provide a more useful comparison to the substrate-gated 2D FET.

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thickness (EOT) of the gate stack in the 2D NC-FET. Before calculating the EOT, it should be noted that the permittivity of the P(VDF-TrFE) ε_P is strongly dependent on the polarization of the polymer, with ε_P reaching the thousands when fully ferroelectrically polarized. Here, we are assuming that such ferroelectric polarization has not been achieved and have used the permittivity of the polymer as given by the manufacturer.[36] The EOT of the gate stack is calculated to be ~79.6 nm through a comparison of the dielectric constant (~9 for Al_2O_3 and 11 for P(VDF-TrFE)) and respective thickness of the materials to the dielectric constant and equivalent oxide thickness of SiO_2

$$EOT = \varepsilon_{SiO_2}\left(\frac{t_{Al_2O_3}}{\varepsilon_{Al_2O_3}} + \frac{t_P}{\varepsilon_P}\right), \quad (3)$$

where ε_{SiO2} is the SiO_2 dielectric constant, t_{Al2O3} is the thickness of the Al_2O_3, ε_{Al2O3} is the Al_2O_3 dielectric constant, t_P is the P(VDF-TrFE) polymer thickness, and ε_P is the P(VDF-TrFE) dielectric constant. In other words, in the purely electrostatic picture, the substrate gate (EOT $\approx$ 10 nm) should have offered better control of the MoS_2 channel (resulting in lower SS) than the ferroelectric/dielectric top gate stack (EOT $\approx$ 79.6 nm).

To reconcile the degradation occurring at the polymer-dielectric interface, an interfacial metal layer was added between these layers of the gate stack, as shown in the full process flow in Fig. 3. The additional gate keeps the ferroelectric-dielectric interface from interfering with the spontaneous polarization occurring in the ferroelectric P(VDF-TrFE), allowing for a more stabilized NC effect and thus sub-60 mV/dec switching over a wide span of drain current I_d. The interfacial metal layer also provided the ability to monitor the electrical characteristics of the top-gated 2D FET with Al_2O_3 as the gate dielectric, affording a second comparison to the baseline, substrate-gated 2D FET, and the final 2D NC-FET (see Fig. S1). The interfacial metal layer was carefully positioned between the source and drain contacts using electron beam lithography to allow the gate to maintain control of the device.

Comparison of the top-gated 2D NC-FETs with the interfacial metal layer and the substrate-gated 2D FETs of the same MoS_2 channel and contacts is given in Fig. 4. There are several key observations from these 2D NC-FET devices. First, the clear and substantial reduction in SS down to 11.7 mV/dec and 14.4 mV/dec in the 1 μm and 500 nm channel length devices, respectively. These SS improvements extend over 3–4 orders of magnitude in I_d, indicating a substantial spontaneous amplification of the applied gate potential in modulating the surface potential of the MoS_2 (ψ_s)—an achievement that is aided by the more steady capacitance of the ultrathin 2D MoS_2 channel.[37] Another key observation is related to the gate leakage current I_g, as shown in Figs. 4(e) and 4(f). Any time a device exhibits a sudden and dramatic drop in I_d, it is crucial to ensure that it is not a result of leakage currents; in the present case, the leakage current remains both low and steady throughout the subthreshold region thus indicating that the observed SS is not based on a gate leakage behavior. The next observation is the negative shift in threshold voltage for both of these 2D NC-FETs compared to their substrate-gated counterparts. There are a variety of factors that could influence this shift, most impactful of which is the presence of charge traps and fixed charge introduced by the ALD grown Al_2O_3 gate dielectric. Evidence of this being

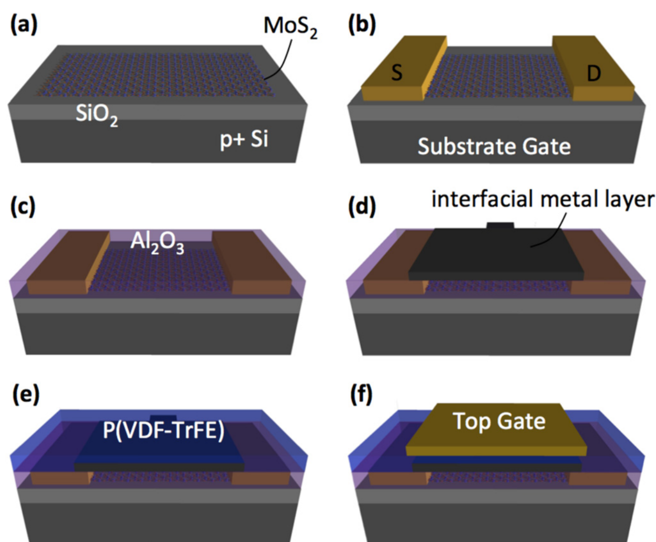

FIG. 3. Schematic process flow for fabricating 2D NC-FETs with an interfacial metal layer between the ferroelectric and dielectric, including: (a) mechanically exfoliate MoS_2 on heavily p-doped Si with 10 nm thermally grown oxide, (b) establish source/drain contacts of Ni to form substrate-gated MoS_2 2D-FET, (c) deposit 20 nm Al_2O_3 gate dielectric using ALD, (d) pattern and deposit interfacial metal layer of 50 nm Au, (e) spin coat P(VDF-TrFE) layer, and (f) establish top gate of Ti/Au to complete the top-gated 2D NC-FET with interfacial layer.

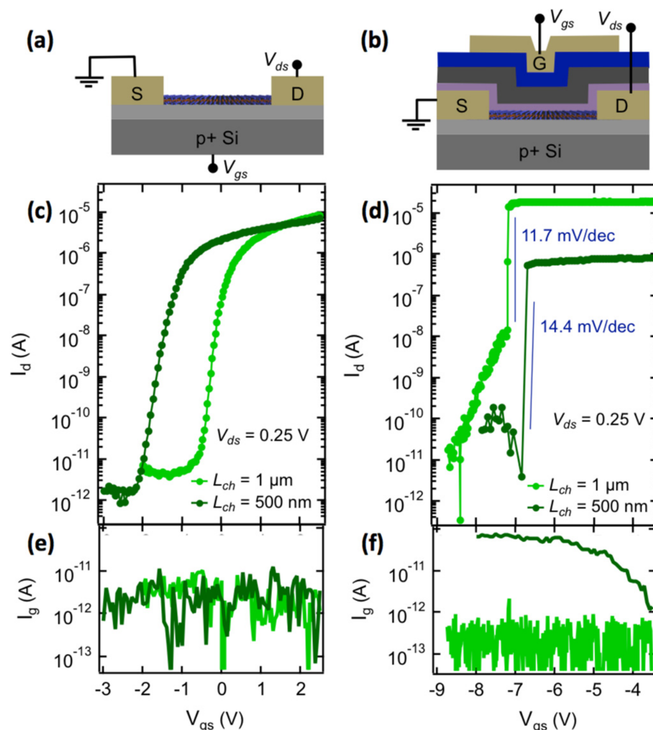

FIG. 4. Schematics of the characterization configuration for (a) substrate-gate 2D FETs and (b) top-gate 2D NC-FETs with the interfacial metal layer. Comparative subthreshold curves from devices (c) substrate-gated and (d) top-gated show the dramatic improvement in subthreshold swing achieved with the NC gate stack. The devices in (c) and (d) are using the same MoS_2 channel and contacts at the indicated channel length L_{ch}. Gate leakage current for the devices in (c) and (d) is provided in (e) and (f), respectively.

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the primary cause of the threshold voltage shift is seen in the comparison of subthreshold curves for a device operated with the substrate gate, interfacial metal gate, and top gate (see Fig. S2), wherein operation with the interfacial metal gate (top gate with Al_2O_3 but no ferroelectric) already results in a negative threshold voltage shift of approximately 12 V. A final observation is that there is an inconsistent change in the on-current for these 2D NC-FETs compared to their substrate-gated operation: the 1 μm device showing an increase while the 500 nm device has a decrease. This impact on the on-current is under further investigation and at the very least these present results show that an on-current boost is indeed possible. It is important to note that the overall results for these 2D NC-FETs in terms of SS improvement are consistent with what has previously been observed with Si-based NC-FETs, where the subthreshold swing has been reduced over a localized range of gate-modulated drain current.[11,14,38–40]

The considerable improvement in SS for these 2D NC-FETs is promising but unstable. All of the devices that exhibited the behavior shown in Fig. 4(d) immediately degraded upon further characterization. Such breakdown is not a unique observation for the polymeric ferroelectric.[5,30,31,41] Unfortunately, this breakdown made it impossible to study the hysteresis behavior in these 2D NC-FETs as the return sweep of the reported curves already showed the degraded behavior (see Fig. S3). While the use of the ferroelectric-dielectric gate stack with an interfacial metal layer has been shown to suppress hysteresis, the present devices do not allow for such postulation to be validated. Aside from rendering it impossible to obtain more detailed characterization data from the devices, this breakdown of the ferroelectric behavior in the P(VDF-TrFE) is obvious evidence for its unreliability for use in a FET technology. While it worked well in providing this initial result of sub-60 mV/dec switching in 2D NC-FETs, future work should make use of the more technologically relevant and reliable doped-HfO_2 ferroelectrics, such as $HfZrO_2$, which has seen tremendous advancement in the last few years.[42–44] Unlike P(VDF-TrFE), doped-HfO_2 ferroelectrics are CMOS process compatible (through atomic layer deposition) and exhibit a highly reproducible increase in ferroelectric response with decreasing film thickness (hence, scalability), with extensive cycling stability. These point toward doped-HfO_2 films as a much more reliable ferroelectric option than P(VDF-TrFE) for stabilized NC-FET devices. Integration of the doped-HfO_2 with 2D channel materials will be a focus for future studies so as to combine the benefits of an ultrathin channel with a robust negative capacitance effect.

In summary, incorporating 2D MoS_2 as the channel material in negative capacitance FETs has been shown to enable subthreshold swings well below the thermal limit (down to 11.7 mV/dec) that extend over several orders of magnitude in drain current. The inclusion of an interfacial metal layer between the polymeric ferroelectric and gate dielectric proved crucial to realizing sub-60 mV/dec switching. Rather than electrically adding a separate ferroelectric capacitor in series with a 2D FET, the ferroelectric was integrated into the gate stack for these devices. While this enabled demonstration of superb low voltage switching behavior, the P(VDF-TrFE) ferroelectric polymer proved to be unstable beyond initial testing. Going forward, further exploration of the use of 2D nanomaterials in NC-FETs with more stable and technologically-compatible ferroelectrics should be pursued for their ability to yield near-ideal switching over a wide extent of drain current.

See supplementary material for detailed fabrication processes and further 2D NC-FET characterization data including threshold voltage shift.

We are grateful to Radiant Technologies for assistance obtaining polarization vs. electric field data. This work was performed in part at the Duke University Shared Materials Instrumentation Facility (SMIF), a member of the North Carolina Research Triangle Nanotechnology Network (RTNN), which is supported by the National Science Foundation (Grant ECCS-1542015) as part of the National Nanotechnology Coordinated Infrastructure (NNCI). F.A.M. acknowledges support from the National Science Foundation (NSF) through the NSF Graduate Research Fellowship under Grant No. DGF 1106401.

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