Realizing ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ with elemental capping layers

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Hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$ or HZO) thin films show great promise for enabling ferroelectric field-effect transistors (FeFETs) for memory applications and negative capacitance FETs for low-power digital devices. One challenge in the integration of ferroelectric HZO is the need for specific capping layers to yield the most pronounced ferroelectric behavior; to date, superior HZO devices use titanium nitride or tantalum nitride, which limits HZO integration into various device structures. In this work, the authors demonstrate the use of elemental capping layers, including Pt, Ni, and Pd, for driving ferroelectricity in HZO. Different combinations of these capping metals, along with changes in the HZO thickness and annealing conditions, have yielded the optimal conditions for maximizing ferroelectric behavior. A remnant polarization of 19 $\mu C/cm^2$ and a coercive field strength of 1.07 MV/cm were achieved with the Pt/HZO/Ni stack annealed at 650 °C with a HZO thickness of ~20 nm. These results bring even greater promise to the use of HZO in memory and/or digital electronic devices by expanding the toolkit of materials that may be used for realizing ferroelectricity. *Published by the AVS.* https://doi.org/10.1116/1.5002558

I. INTRODUCTION

Variations of hafnium oxide (HfO_2) have been widely employed for gate dielectric thin films in the electronics industry for metal-oxide-semiconductor field-effect transistors (MOSFETs). Recently, it has been reported that the doping of HfO_2 with appropriate metals can yield ferroelectricity under certain conditions,[1,2] thus showing potential for revolutionizing the field of energy-efficient digital and nonvolatile memory devices.[3,4] Nonvolatile memory devices with ferroelectric thin films, such as ferroelectric random access memory devices and ferroelectric field-effect transistors (FeFETs), have traditionally focused on perovskite materials, which require thick films to avoid large leakage currents due to their small bandgap and low barrier height.[5,6] Therefore, the discovery of ferroelectricity in doped-HfO_2 thin films with a nanometer-scale thickness was a boon for the miniaturization of memory devices at advanced technology nodes. In addition to memory devices, ferroelectrics also showed promise for use in low-power digital devices aimed at overcoming the thermal limit for switching of MOSFETs.[7–10] The development of negative capacitance field-effect transistors (NC-FETs), which exploits a ferroelectric material to achieve an effective negative capacitance when properly integrated into a transistor gate stack, has proven to be a promising path to lower operating voltage as a sub-60 mV/decade switch.[11–15] The encouraging demonstration of ferroelectricity in doped-HfO_2 films has accelerated research into NC-FETs as the ferroelectric metal-oxide films are compatible with CMOS processing.[16–18]

Most prominent of the doped-HfO_2 ferroelectric films is hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$ or HZO), which offers several benefits, including enhanced polarization at scaled thicknesses compared to traditional ferroelectrics (e.g., polymeric compounds and perovskites).[19–21] Additionally, HZO requires lower annealing temperature for conversion to a ferroelectric crystal structure and is simple to fabricate using atomic layer deposition (ALD), benefiting large-scale industrial production.[22,23] However, the application of HZO into various device structures, such as integration with 2D semiconducting channel materials, requires appropriate capping layers to address the difficulty of nucleating ALD films on these inert nanomaterial surfaces and the sensitivity of the nanomaterials to exposure in the ALD growth environment.[22] Beyond these integration challenges, there are also the benefits that can come from having access to a wide variety of gating electrode materials (which are the capping layer electrodes in the metal-ferroelectric-metal (MFM) when integrated into a NC-FET or FeFET), as the properties (e.g., work function) of these electrodes will influence the operation of the resulting FET devices, by setting parameters such as threshold voltage. Therefore, a wider range of capping layer materials available for achieving ferroelectric HZO will increase the degrees of freedom needed for integration into advanced NC-FETs and FeFETs, where there are other sensitivities and limitations to processing conditions that would benefit from a wider range of options.[10,24] For instance, the use of elemental capping layers: (1) eliminates further etching processes for patterning ALD deposited films (i.e., lift-off processes can be used), (2) expands the material options for specific device applications (e.g., choosing electrodes with specific work functions for setting threshold voltage), and (3) makes possible the formation of better interfaces with the underlying substrate.

Ferroelectricity in HZO is exhibited in the orthorhombic crystal phase. In order to form the orthorhombic structure, capping layers are preferred as they provide mechanical confinement that inhibits shearing of the crystal unit cell, thus

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suppressing the monoclinic phase while enabling a transition to the orthorhombic phase.[25] While many research groups have demonstrated ferroelectricity with ALD or sputtered titanium nitride (TiN) and tantalum nitride (TaN) electrodes, the influence of other capping layers and their ability to drive ferroelectricity in HZO still need to be investigated.[1,10,26] A few studies that explore capping layers for HZO outside of TiN or TaN have included Ni/HZO/Ru/Si,[27] TiN/HZO/Pt,[28] and TiN/HZO/RuO_2,[29] and Ir/HZO/TiN.[30,31] Ferroelectric performance of these capping layers was significantly less than those with TiN or TaN exclusively, except for a recently published paper exploring the use of a tungsten electrode, W/HZO/SiO_2, with minimal diffusion of W into HZO.[32] Thus, there remains a need for developing other capping layers that are compatible with new device structures without significant compromise of the ferroelectric performance.

In this work, we demonstrate ferroelectric behavior of MFM capacitors using different combinations of Pt, Ni, and Pd elemental metal capping layers. A parametric study of the impact of thermal annealing conditions and the HZO thickness is carried out for each capping layer arrangement, providing insight into the most favorable combination of bottom and top layers. HZO was grown using ALD, and capping layers were formed using standard physical vapor deposition processes. The highest values for remnant polarization (P_r) and coercive field strength (E_c) reach 19 $\mu C/cm^2$ and 1.07 MV/cm, respectively, for the Pt/HZO/Ni stack annealed at 650 °C for 30 s with 20 nm thick HZO, showing performance that is competitive with TiN- or TaN-capped HZO. These results expand the options for integration of this promising ferroelectric into technologically viable memory and low-voltage digital transistors by using metal electrodes other than TiN or TaN to achieve greater ferroelectricity in HZO.

II. EXPERIMENT

The MFM capacitor is composed of two separate metal capping layers (in this article, "capping layers" refer to both top and bottom electrodes) in a parallel-plate. The capacitors were fabricated on Si wafers with 10 nm thermally grown SiO_2 with both top and bottom electrodes patterned using photolithography and deposited using electron-beam evaporation with a thickness of 20 nm. ALD was employed to deposit the HZO films at 270 °C, using tetrakis(ethylmethylamino)hafnium {$Hf[N(C_2H_5)CH_3]_4$} and tetrakis(ethylmethylamino)zirconium(IV) {$Zr[N(C_2H_5)CH_3]_4$} as the Hf and Zr precursors, respectively. Water vapor was used as the oxidant and argon (Ar) as the purge and carrier gas. Thicknesses of 5–25 nm HZO films were deposited with a Hf:Zr ratio of 1:1 by alternating ALD cycles of HfO_2:ZrO_2, with pulse and purge times of 200 and 20 000 ms, respectively. These conditions yielded a growth of 0.15 nm/cycle for the HZO films, as verified by ellipsometry. A top electrode was deposited by electron beam evaporation, forming the parallel-plate MFM structure shown in Fig. 1(a). Rapid thermal annealing in a nitrogen ambient was carried

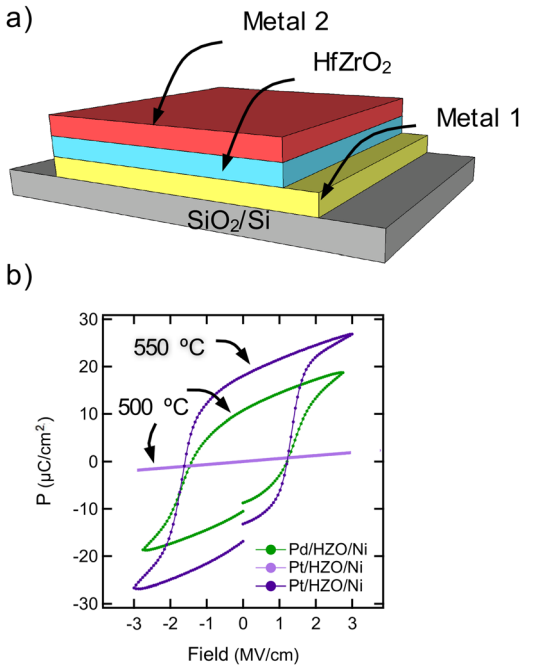

FIG. 1. (Color online) MFM structure and the impact of annealing temperature on ferroelectric behavior. (a) Schematic of parallel-plate MFM capacitors with the structure of metal 1/HZO/metal 2. Metals 1 and 2 refer to the bottom and top electrodes, respectively. (b) P-E curves of Pt/20 nm HZO/Ni and Pd/20 nm HZO/Ni demonstrating how the temperature for driving ferroelectric behavior depends on the capping layer stack.

out for all devices for 30 s at different temperatures, from 500 to 900 °C. The crystallographic phase of the HZO films was analyzed using grazing-angle incidence x-ray diffraction (GAXRD) (Panalytical X'Pert PRO System). For electrical characterization (using a Radiant RT66B), polarization–electric field (P-E) hysteresis loops were obtained at room temperature with a 1 kHz triangular-wave electric field, after applying a cycling voltage of ±5 V for 1 s to enable characterization of the devices in order to eliminate any "wake up effect" commonly observed in HfO_2 thin films.[33–36] Endurance tests were performed at 1 kHz with an applied voltage of 4 V up to 5×10^4 cycles as the curve eventually turns flat.

III. RESULTS AND DISCUSSION

The impact of annealing temperature on driving ferroelectric behavior in the MFMs with various capping layers was analyzed using hysteretic P-E curves, as shown in Fig. 1(b). Without annealing, a simple linear P-E response was obtained, while annealing at elevated temperatures resulted in a hysteresis loop, indicating ferroelectric behavior. This degree of temperature, however, is dependent on the capping layer stack. As demonstrated in Fig. 1(b), the minimum annealing temperature required to achieve ferroelectric behavior for Pd/HZO/Ni was 500 °C, while Pt/HZO/Ni required 550 °C before it became ferroelectric. Although Pt and Pd have a similar face-centered cubic structure, they may offer different conditions for the growth behavior of the HZO film, resulting in different in-plane strains, thus influencing the subsequent transition to the ferroelectric orthorhombic phase.[22,25] Therefore, tailoring different capping layer combinations enables the adjustment

of annealing temperature for ferroelectricity, allowing the integration of HZO into various kinds of FETs for meeting different processing requirements.

Hysteresis loops for MFM capacitors with 20 nm thick HZO were influenced by both annealing temperature (from 500 to 750 °C) and capping layers. MFM capacitors with Pd/HZO/Pt, Pd/HZO/Ni, and Pt/HZO/Ni were fabricated and tested for each of the conditions [Figs. 2(a)–2(d)]. The impact of annealing temperature on P_r was very subtle for the Pd/HZO/Ni stack [Fig. 2(a)]; yet, for Pt/HZO/Pd [Fig. 2(b)], P_r increased steadily with increasing annealing temperatures from 500 to 700 °C. In contrast, the other two MFM capacitors of Pt/HZO/Ni [Fig. 2(a)] and Pd/HZO/Ni [Fig. 2(c)] displayed increasing polarization with increasing annealing temperature until the maximum polarization at 650 °C [Fig. 2(d)]. The MFM stack of Pt/HZO/Ni also yielded the highest polarization (19 μC/cm^2) at 650 °C. The lowest point of P_r matches the observation of the annealing temperature required for ferroelectricity, as the temperature of inducing ferroelectric behavior in Pd/HZO/Ni is 500 °C, while that for Pt/HZO/Ni and Pd/HZO/Pt is 550 °C [Fig. 2(d)]; as a clarification, the low P_r at 500 °C shown in Fig. 2(d) for both Pd/HZO/Pt and Pt/HZO/Ni represents linear capacitor behavior.

The effect of the HZO thickness (from 10 to 25 nm, with an increment of 5 nm) under varying annealing conditions for Pd/HZO/Ni MFM capacitors was also investigated. The polarization was very sensitive to the change in the HZO thickness. Devices with 10 nm thick HZO exhibited a linear response in P-E curves from 0 to 600 °C. Devices with 15 nm HZO also did not show ferroelectric behavior, even at an elevated temperature of 700 °C. HZO films of 20 nm or more exhibited ferroelectric behavior and larger polarizations, with thicker films (25 nm compared to 20 nm), resulting in higher polarization values with 600 °C annealing, while the ones annealed at 750 °C presented degraded performance [Figs. 3(a) and 3(b)]. Typically, thinner films ~10 nm of HZO yield greater P_r.[37] However, in this study, devices with 10 and 15 nm thick HZOs are prone to become resistive compared to 20 nm thick HZO, as leakage current paths tend to develop along the grain boundaries in former devices.[17]

Retention and fatigue tests of Pd/20 nm HZO/Ni and Pt/20 nm HZO/Ni MFM stacks annealed at 700 °C demonstrated the potential of HZO in memory devices, as shown in Figs. 4(a) and 4(b). In the retention tests, repeated read/write operations were performed for samples at voltage levels of 4 V. All samples showed similar trends of strong retention over ~700 cycles [Fig. 4(a)]. However, in the fatigue test, switching polarization exhibited a significant drop in the first 10^4 cycles, leveling out after 2×10^4 cycles [Fig. 4(b)]. As a reference, the HZO capped with TiN layers in a FeFET device lasted ~10^4 cycles in endurance testing,[37] proving that the Pd/HZO/Ni and Pt/HZO/Ni MFM stacks in this work showed comparable fatigue performances that stimulate more extensive research for their integration into memory applications. Compared to ferroelectric thin films based on Si-doped HfO_2, which sustained up to 10^{10} cycles, HZO requires more improvement on endurance characteristics.[37]

Evidence of the formation of the orthorhombic phase for the Pt/20 nm HZO/Ni MFM was observed using GAXRD [Fig. 4(c)]. Before annealing, the GAXRD peaks showed a slight mixture of (111_m) monoclinic and (111_o) orthorhombic phases, as commonly observed in previous studies.[1,2] After annealing at 600 and 650 °C, the peak intensity of the (111_o) crystal orientation is increasingly more prominent, indicating the formation of the orthorhombic phase through atomic rearrangement of the film during annealing.[1,26] This transition, including the relative increase in peak intensity with annealing temperature, is consistent with the P-E results that show the impact of annealing conditions on driving ferroelectric behavior. Another effect of increasing the annealing temperature from 600 to 650 °C is an increase in the intensity of the (111_o) peak at 30.56°, suggesting that annealing at higher temperature increases the portion of orthorhombic phases and decreases that of the monoclinic phase.

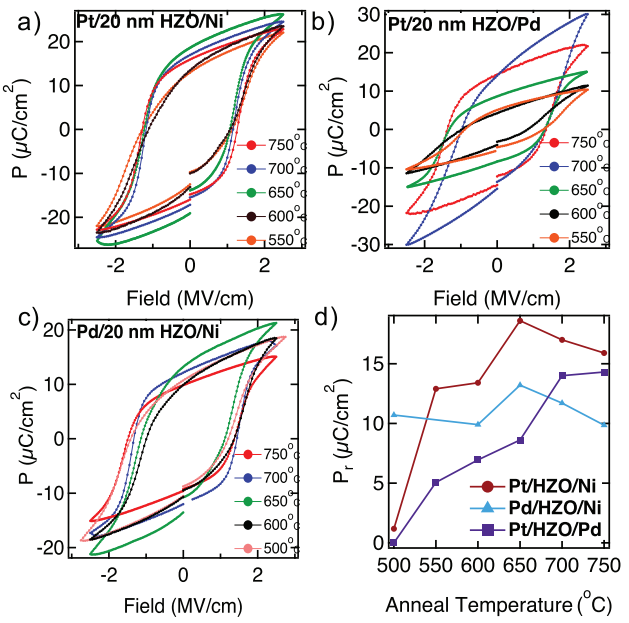

FIG. 2. (Color online) P-E curves from MFM capacitors with different metal capping layer stacks, annealed at various temperatures. The MFM stacks are (a) Pt/20 nm HZO/Ni, (b) Pt/20 nm HZO/Pd, and (c) Pd/20 nm HZO/Ni. (d) Average P_r vs annealing temperature from Pt/HZO/Ni, Pt/HZO/Pd, and Pd/HZO/Ni with a HZO thickness of 20 nm.

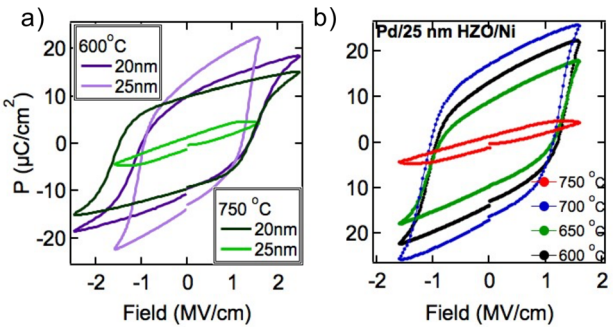

FIG. 3. (Color online) Postanneal P-E curves at various annealing temperatures from MFM capacitors comprised of Pd/HZO/Ni with varying HZO thicknesses of (a) 20 and 25 nm and (b) 25 nm.

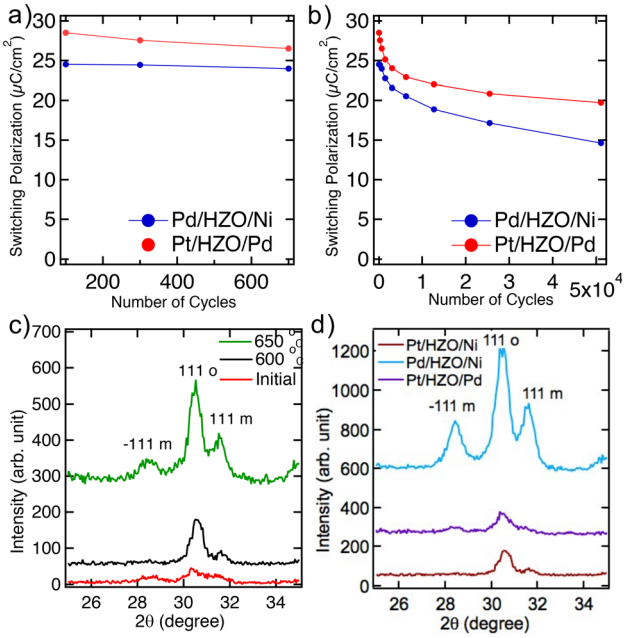

FIG. 4. (Color online) (a) Retention and (b) fatigue testing at 1 kHz with an applied voltage of 4 V for Pd/20 nm HZO/Ni and Pt/20 nm HZO/Pd MFM capacitors annealed at 700 °C. (c) GAXRD for Pt/20 nm HZO/Ni initially and after different annealing temperatures. (d) GAXRD for Pt/20 nm HZO/Ni, Pd/20 nm HZO/Ni, and Pt/20 nm HZO/Pd MFM capacitors.

Although a clear determination of the orthorhombic and tetragonal phase is not possible from direct measurements due to their similar 2 theta values, the existence of ferroelectricity in these MFMs originates from the non-centro-symmetric orthorhombic phase rather than the centro-symmetric tetragonal phase.[28]

The GAXRD results offer insight into the temperature trend of the P_r characteristics. The significant rise in P_r from 13 to 19 μC/cm^2 for Pt/HZO/Ni due to the annealing temperature increase (600 to 650 °C) [Fig. 2(d)] is a result of the formation of a higher portion of the orthorhombic phase as confirmed by the GAXRD result [Fig. 4(c)]. Also, the crystal structures of various MFM capacitors annealed at 600 °C, including Pt/20 nm HZO/Ni, Pd/20 nm HZO/Ni, and Pt/20 nm HZO/Pd, were investigated using GAXRD [Fig. 4(d)] and explained by the relative ratio of $(111_o)/\{(111_o)+(111_m)+(-111_m)\}$. The relative ratio for Pt/20 nm HZO/Ni, Pd/20 nm HZO/Ni, and Pt/20 nm HZO/Pd was 55%, 50%, and 59%, respectively, indicating that differences in the orthorhombic phase formation contribute to different ferroelectric behaviors.

The impact of various capping layer combinations and annealing conditions on the ferroelectric properties of HZO-MFM capacitors is summarized in Table I. Without thermal annealing, all devices had a linear response in the P-E curve, which is indicative of standard linear capacitors. Only after exposure to sufficient annealing temperatures did the devices show ferroelectric behavior. The temperature at which HZO exhibited ferroelectricity varying between different capping layers. The Pd/HZO/Ni capacitor displayed ferroelectricity at 500 °C, which was lower than that of both Pt/HZO/Ni and Pd/HZO/Pt stacks; hence, the use of Pt capping layers leads

TABLE I. Ferroelectric behavior of 20 nm HZO with different metal capping layers.

T (°C)	Pt/HZO/Ni	Pd/HZO/Ni	Pd/HZO/Pt
0	N[a]	N	N
500	N	FE	N
550	FE[b]	FE	FE
600	FE	FE	FE
650	FE	FE	FE
700	FE	FE	FE
750	FE	FE	FE

[a]N: a linear capacitor, nonferroelectric.
[b]FE: ferroelectric behavior.

to a slightly higher annealing temperature requirement for HZO to display ferroelectricity. All devices became resistive above annealing temperatures of ~800 °C, which was observed in other work and was attributed to current leakage paths developed along the grain boundaries.[17] The effect of the HZO thickness (from 5 to 25 nm, with an increment of 5 nm) under varying annealing conditions for Pd/HZO/Ni MFM capacitors was also studied but is not included in the table. Only the devices with HZO thicker than 20 nm displayed ferroelectric behavior, but the data were inconclusive regarding whether this was directly related to the capping layers or the deposited HZO film uniformity and quality.

Comparison of the ferroelectric performance in the present MFM devices with previous studies using other capping layers with HZO is shown in Table II. Compared to the TiN and Ru/Ni capping layers,[22,27] Pt/HZO/Ni with a HZO thickness of 20 nm in this work shows the largest P_r of 19 μC/cm^2 at annealing conditions of 650 °C, demonstrating superior polarization behavior and strong feasibility for memory device applications. Meanwhile, E_c is relatively lower than those of TiN and Ru/Ni capping layers.[22,27] This may be due to the fact that the high work function nature of the elemental electrodes used in this study presented a more substantial barrier to oxidation than those of TiN and Ru/Ni. Thus, the lack of the formation of additional oxide "dead-layers" at the electrode interfaces resulted in decreased E_c.[36]

IV. SUMMARY AND CONCLUSIONS

In summary, we have successfully established greater ferroelectric properties for HZO with new elemental metal capping layers, including Pd/HZO/Pt, Pd/HZO/Ni, and Pt/HZO/Ni, expanding the options for using HZO films in various low-power digital or memory devices. The influence of the HZO

TABLE II. Comparison with previous studies on ferroelectric performance of various capping layers with HZO. Pt/20 nm HZO/Ni shows the largest P_r of 19 μC cm^{-2} at annealing conditions of 650 °C.

Capping layers	TiN/HZO/TiN (Ref. 22)	Ru/HZO/Ni (Ref. 27)	Pt/HZO/Ni (this work)
Thickness (nm)	10	25	20
Temperature (°C)	600	550	650
P_r (μC cm^{-2})	15	6	19
E_c (MV cm^{-1})	1.7	2.4	1.07

thickness, capping layer materials, and annealing temperature on the ferroelectric behavior was studied. Compared to other MFM capacitors from HZO, Pt/HZO/Ni with 20 nm HZO annealed at 650 °C yielded the highest P_r of 19 μC/cm^2 with E_c of 1.07 MV/cm. The insights presented in this study provide new ways to integrate ferroelectric HZO thin films into technologically viable memory and low-voltage digital transistors.

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