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Effects of Gate Stack Composition and Thickness in 2-D Negative Capacitance FETs

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ABSTRACT Negative capacitance (NC) field-effect transistors (FETs) with 2-D semiconducting channels have become increasingly attractive due to their ability to produce sub-60 mV/dec switching behavior in a physically scalable device. However, it has yet to be determined how gate control, including threshold voltage, of 2-D NC-FETs is impacted by gate dielectric composition, along with dielectric and ferroelectric layer thicknesses. Here, we show the threshold voltage shifts positively under increasing ferroelectric thickness and negatively with increasing dielectric thickness. This shifting behavior is observed in devices without an interfacial metal layer between the ferroelectric hafnium zirconium oxide ($HfZrO_2$ or HZO) and dielectric. Because the interface between the ferroelectric and dielectric is critical in driving NC behavior, we also study 2-D NC-FETs with 4 nm HZO paired with different dielectrics. These results reveal that the HZO/Al_2O_3 interface is more favorable than either the HZO/ZrO_2 or HZO/HfO_2 interfaces. Finally, the impact of an interfacial metal layer is discussed by comparing the 2-D NC-FET performance of similar devices with and without this layer.

INDEX TERMS Negative capacitance, two-dimensional, 2D, NC, 2D FET, NC-FET, hafnium zirconium oxide, ferroelectricity.

I. INTRODUCTION

Lately, there has been a surge of research activity around negative capacitance field-effect transistors (NC-FETs) that use doped hafnium oxide thin films as the ferroelectric due to the numerous benefits of this material, such as CMOS compatibility and increased ferroelectric response at scaled thicknesses [1]–[9]. Many devices employing HZO have incorporated a metallic interfacial layer into the design to mitigate any adverse interfacial effects and to eliminate the emergence of a passive layer that suppresses ferroelectricity [1]–[3], [10]–[12]. Recently, it was discovered that the metallic layer introduces an overlap capacitance and depolarization field that adversely affect device performance [13], leading some researchers to investigate NC-FETs without an interfacial layer [5], [14]–[16]. However, understanding of how the ferroelectric and dielectric layers without an interfacial metal influences the negative capacitance behavior has yet to be determined with experimental evidence. This has become of particular importance for NC-FETs with 2D semiconductors as the channel (2D NC-FETs), where there is considerable difference in device performance based on the composition and thickness of the gate stack layers and presence or absence of an interfacial metal [3], [5], [9], [16]–[19].

The performance of NC-FETs involves gate-control, which relates to better capacitance matching with the ferroelectric. To achieve sub-60 mV/dec operation and avoid instability in NC-FETs, it is crucial that the negative differential capacitance of the ferroelectric ($C_{FE} < 0$) compensates the positive capacitances ($C_{dev} > 0$) in the device such that the resulting gate capacitance, $C_G = (C_{FE}^{-1} + C_{dev}^{-1})^{-1}$ can be made larger than C_{dev} [20]. The maximum enhancement

of capacitance is feasible when C_{FE} is matched to C_{dev} ($-C_{FE} = C_{dev}$ and $-C_{FE} > C_{dev}$). This scenario of capacitance matching is influenced by dielectric constants in different dielectric oxides, and can be tuned by changing the thickness of the films. In this work, we examine experimental data from bottom-gated 2D NC-FETs without a metallic interfacial layer to investigate the effects of dielectric material composition, as well as ferroelectric and dielectric oxide thickness, on the operation and performance of the devices. First, the dielectric type and thickness was fixed and different ferroelectric thicknesses were studied. Then, the ferroelectric thickness was fixed while varying dielectric type and thicknesses were explored. This systematic approach revealed a strong threshold voltage dependence on layer thicknesses and the preferential performance of the HZO/Al_2O_3 interface.

II. DEVICE FABRICATION

HZO films were grown on p++ Si wafers using atomic layer deposition (ALD), followed immediately by ALD growth of a dielectric oxide. Samples were then annealed at 550°C for 30 s with rapid thermal annealing (RTA) to drive the ferroelectric transition of the HZO. Molybdenum disulfide (MoS_2) was mechanically exfoliated and transferred onto each wafer, and the thicknesses of the MoS_2 flakes used were confirmed with atomic force microscopy (AFM) to be 3-7 nm. It is important to note that the thickness range of our channels is not substantial enough to noticeably affect the gate control. This can be verified by calculating the approximate electrostatic screening length for the devices [21]. For the extremes of 3 nm and 7 nm body thickness of MoS_2, the approximate screening lengths are around 6 and 9 nm, respectively. Hence, electrostatic control will not be compromised by this range of body thickness. After the wafers were coated with poly(methyl methacrylate) (PMMA), the source/drain contacts were patterned with electron beam lithography (EBL) and metallized with 20 nm Ni in an electron beam evaporator. Following lift-off in acetone, the wafers were again coated with PMMA and contact pads were written with EBL and metallized with 2 nm Ti/10 nm Pd/20 nm Au.

Each device used to study the effects of ferroelectric thickness on the 2D NC-FET had 6, 12, or 18 nm HZO with 10 nm HfO_2. The devices used to determine the effects of dielectric thickness were fabricated with 12 nm HZO and 5, 10, or 15 nm HfO_2. The schematics of each device set are shown in Fig. 1(a,d). The devices constructed to investigate the effects of oxide composition were fabricated with 4 nm HZO with 4 nm of either Al_2O_3, HfO_2, or ZrO_2. All devices were electrically characterized with an Agilent (Keysight Technologies) B1500A Semiconductor Parameter Analyzer, using the same measurement conditions as previous publications in the field for consistency [3]. Standard I_d-V_{gs} sweeps were performed at measurement lengths of 10 μs corresponding to sweep rates of 11.90 Hz.

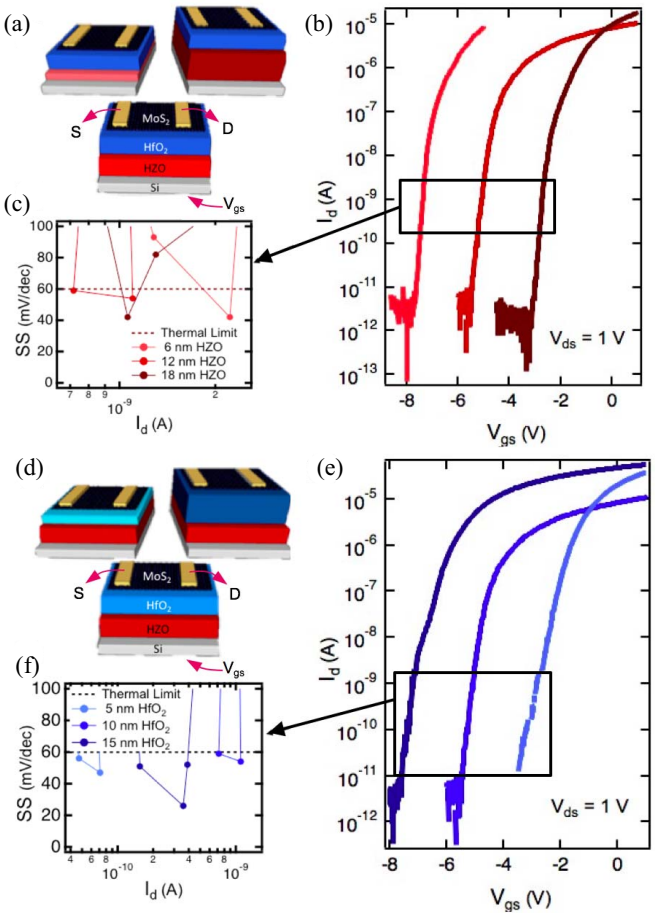

FIGURE 1. Impact of ferroelectric and dielectric thickness on 2D NC-FETs. (a) Schematics of device structures detailing the increasing HZO thickness. (b) Subthreshold curves showing a positive threshold voltage shift with increasing HZO thickness (HfO_2 fixed at 10 nm), and (c) subthreshold swing (SS) from the region of sub-60 mV/dec behavior. (d) Schematics, (e) subthreshold curves, and (f) SS for the HfO_2 thickness scaling devices (HZO fixed at 12 nm). All devices have L_{ch} = 500 nm.

III. RESULTS AND DISCUSSION

The dependence of the threshold voltage on the ferroelectric and gate dielectric thicknesses were independently studied and are displayed in Fig. 1. Figure 1(a-c) shows the effect of modifying the HZO thickness to 6, 12, or 18 nm with a 10 nm HfO_2 gate oxide. The threshold voltages have a consistent positive shift with increasing HZO thickness, from −7 V to −2 V at 18 and 6 nm HZO, respectively, without significantly impacting the overall subthreshold behavior of the 2D NC-FETs (note, the variance in on-state performance is attributed to differences in MoS_2 flake quality, contact interfaces, etc.). Hence, while the thickness of the HZO is known to impact the resultant ferroelectricity, it improves the threshold voltage. The result we observed for the subthreshold behavior is consistent with other simulation work in the field of 2D NC-FETs [5], which also demonstrated improved threshold voltage when increasing the HZO thickness.

As seen in Fig. 1(d-f), devices with a fixed 12 nm HZO ferroelectric layer and three different HfO_2 layer thicknesses,

were also able to achieve a small region of steep switching. In contrast to the impact of the HZO thickness scaling, a pronounced negative shift in the threshold voltage is observed with increasing HfO_2 layer thickness, from approximately -2 to -7 V at 5 and 15 nm, respectively.

The dichotomy in threshold voltage shift between the increasing HZO vs HfO_2 suggests that fixed charge of different polarity is likely present in these films. Typically, HfO_2 has positive fixed charge present owing to oxygen vacancies, which can be ameliorated with annealing [22]. The negative shift in threshold voltage for increasing HfO_2 thickness is consistent with the typical positive fixed charge density. For HZO, the observed positive shift in threshold voltage with increasing film thickness is suggestive of negative fixed charge in the films. However, there are also implications from the tuning of the capacitive network in the devices that may be contributing to the change in threshold voltage. For instance, as the C_{FE} is tuned based on changing HZO thickness, the voltage at which a capacitance matching condition will be realized will be changed owing to the voltage-dependence of contributing capacitances in C_{dev}, such as the quantum capacitance. Hence, further detailed studies will be needed to ascertain the precise source of the threshold voltage shift from changing HZO thickness.

From the results in Fig. 1, the most promising 2D NC-FET behavior (based on threshold voltage nearest to zero and pronounced sub-60 mV/dec switching) arose when the ferroelectric thickness closely matched the dielectric thickness, which should also balance out the threshold voltage shifting being caused by the dissimilar fixed charge and other influences related to thickness changes. Based on this observation, 2D NC-FETs were fabricated with equal ferroelectric and dielectric thicknesses of 4 nm each using three different ALD-grown high-k dielectrics: zirconium oxide (zirconia, ZrO_2), hafnium oxide (hafnia, HfO_2), and aluminum oxide (alumina, Al_2O_3), the results of which are displayed in Fig. 2. As expected, the threshold voltage for all devices, particularly the HZO/HfO_2 device, is relatively close to zero compared to those from the devices in Fig. 1. Part of the interest in investigating scaled devices with only 4nm HZO/4nm dielectric is for their relevance to modern scaled transistor technologies. Four nanometer thick HZO is the thinnest ferroelectric layer integrated into a 2D NC-FET without an interfacial metal to date. The devices with ZrO_2 and HfO_2 (Fig. 2(a,b)) had a much lower on/off-current ratio ($I_{ON} : I_{OFF}$) of 1-2 orders of magnitude, which is attributed to increased leakage currents (up to 10^{-7} A). The primary source of this leakage is gate current owing to the relatively thin overall gate stack of 8 nm compared with the minimum of 15 nm thick overall gate stack for the devices in Fig. 1. Note that this gate leakage incurred from the scaled 4 nm HZO/4 nm dielectric stack is not a fundamental limit to the scaling of this stack; rather, the leakage is also a function of the gate overlap area with the source/drain contacts, which is substantial in these devices. Ultimately, it's clear that at the scaled thickness of 4 nm, both the ZrO_2 and HfO_2 had significantly higher leakage current and lower on-current when compared to the Al_2O_3 dielectric-based devices. The devices with Al_2O_3 had a high $I_{ON} : I_{OFF}$ of > 4 orders of magnitude (Fig. 2(c)) and significantly less gate leakage current by 1-2 orders of magnitude. Further, the switching behavior of the Al_2O_3 device was more stable under changing drain-source bias (V_{ds}) and the on-current was several times greater (more than the standard deviation observed in 2D MoS_2 FETs), both suggesting stronger electrostatic switching and thus a better gate stack compared to the ZrO_2 and HfO_2 devices. It is noted that capacitance matching, which is the critical condition for negative capacitance operation, will be influenced by dielectric constants in these different dielectric oxides. Changing to a higher dielectric constant will increase the C_{dev} and thus require a thinner HZO (lower C_{FE}) to reach the desired matching condition. In our work, the comparison of different dielectrics is made with a fixed 4 nm HZO, therefore, it is reasonable that the dielectric with the lowest permittivity exhibits the best performance. However, there is a multiplicity of other factors, such as different interface trap capacitances, influencing the performance of the devices.

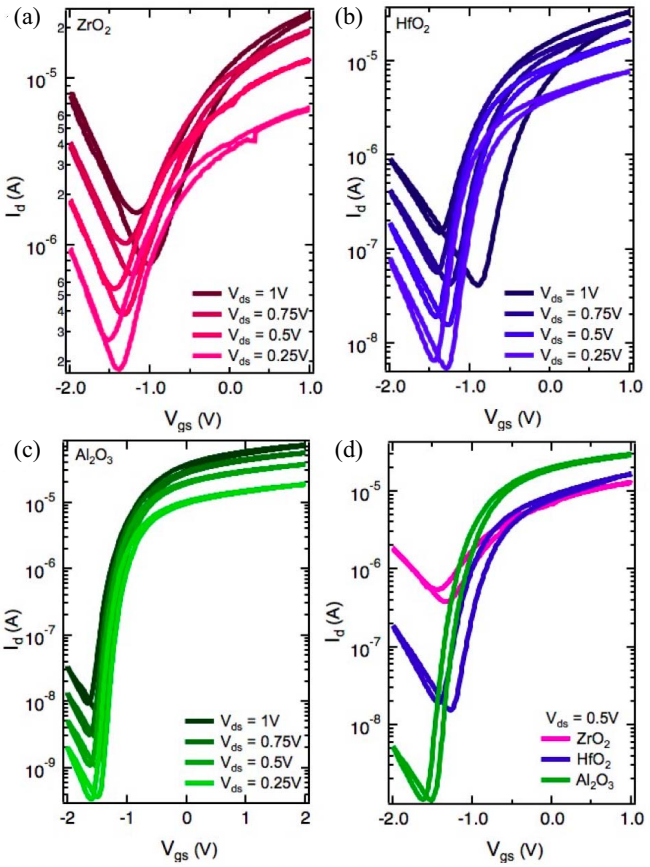

FIGURE 2. Impact of dielectric type on 2D NC-FET performance. Subthreshold curves with small, counterclockwise hysteresis for devices with 4 nm HZO and 4 nm (a) ZrO_2, (b) HfO_2, and (c) Al_2O_3 as the gate oxide at multiple drain biases. (d) Comparative curves for devices at $V_{ds} = 0.5$ V. All devices have $L_{ch} = 500$ nm.

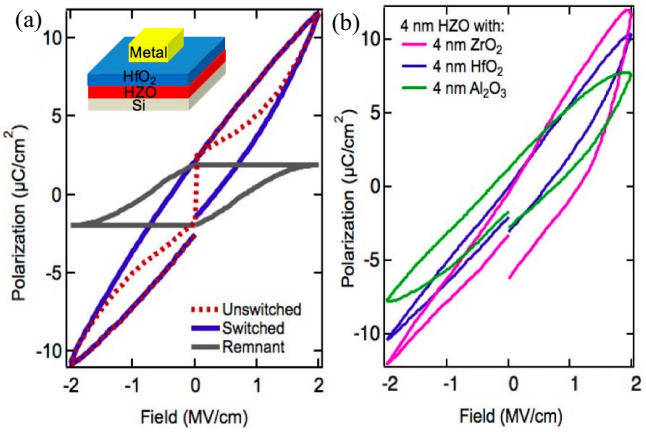

FIGURE 3. Polarization - electric field (P-E) curves for the various gate stacks studied after a 550 °C RTA for 30 secs. The metal used to contact the stacks for collecting the data is 5 nm Ti/20nm Au. (a) Measured polarization of 5 nm HfO_2/12nm HZO excluding the impact of leakage current and (b) polarizations of each 4 nm dielectric with 4 nm HZO. Ferroelectric behavior is demonstrated by the nonlinear polarizations.

Hence, the significance of the results reported is anticipated to prompt the further metrological study of these interfaces in order to better understand and ultimately control them in 2D NC-FETs.

While the Al_2O_3 device showed clear advantages over HfO_2 or ZrO_2, none of the devices with 4 nm HZO produced sub-60 mV/dec switching behavior. This is attributed to three effects: 1) the non-stabilized negative capacitance effect of the HZO stemming from a so-called "passive layer" at the interface between the ferroelectric and dielectric layers [23], [24]; 2) a less favorable capacitance matching scenario [1]; and 3) gate leakage currents that overwhelm the low-current switching regime where pronounced switching may be observed (see Fig. 1). The passive layer arises when variations in the out-of-plane component of the effective permittivity of the ferroelectric create a depolarization field. The depolarization potential across the film is established to ensure an equipotential state in the whole structure. As the potential is related to the spontaneous polarization and the film thickness, the depolarization field will scale accordingly, increasing with decreasing film thickness. As for the capacitance scenario, the unique capacitive behavior of the 2D channel (smaller capacitance, often dominated by voltage-dependent quantum capacitance) in 2D NC-FETs requires thicker HZO in order to enhance the negative capacitance effect for steep SS. The less steep switching behavior for the 4 nm HZO devices is consistent with the simulation results in the field, all showing that the DC voltage gain (body factor) decreases when the ferroelectric thickness decreases for a given V_{GS} [5]. Finally, the gate leakage potentially drowning out the sub-60 mV/dec switching is evident based on the results seen in Fig. 1 where the leakage current was substantially lower and enhanced switching was observed.

The ferroelectric behavior of HZO films used in Figs. 1 and 2 are presented in Fig. 3a and 3b, respectively. The PUND (positive up negative down) method has been employed for excluding the impact of leakage current on the P-E curve (Fig. 3a). The remnant polarization is obtained by removing the un-switched polarization from the switched polarization. The $+P_r$ and $-P_r$ are 1.90 and -1.97 $\mu C/cm^2$, respectively. The resultant lower remnant polarization of HZO than in [3] is related to the absence of the interfacial metal layer, which allows for more effective match between the ferroelectric capacitance and the low channel capacitance by ensuring lower ferroelectric capacitance (low$|dP/dE|$ near $E = 0$) for a given ferroelectric thickness [25]. The more effective match between the ferroelectric capacitance and the low channel capacitance may be the reason of the consistently low hysteresis observed in this work [5].

Comparing the performance of the 12 nm HZO device to that of a previously reported 2D NC-FET with 12 nm HZO sandwiched between TiN interfacial metal layers highlights the pronounced impact of the interfacial metal layers. In this comparison, each device was fabricated so that the thicknesses of the ferroelectric are almost equivalent. The 2D NC-FET with the interfacial layers exhibits significantly improved switching performance, as the interfacial layer compensates for any non-uniformity, such as fixed charges or traps at the interface, thus stabilizing and enhancing the ferroelectric response. Also, an enhanced negative capacitance effect is present for 2D NC-FET with interfacial metal layers due to the larger total capacitance of the capacitor network. This can be explained by assuming the polycrystalline HZO capacitor as many small capacitors in parallel, while these small capacitors of the NC-FET with internal metal are connected from both terminals through the internal metal, those of the NC-FET without internal metal only connect from one terminal. The total capacitance is therefore larger for the NC-FET with internal metal by simple calculations [26]. However, there is also a trade-off in the suppressed on-state modulation in the 2D NC-FET with an interfacial layer, where there is a pronounced drain-side switching phenomena expressed (which is also related to the extensive overlap capacitance in the device), and in the considerable hysteresis present in the device with the interfacial metal. In contrast, the benefit of 2D NC-FETs without the interfacial layers shown in this work has demonstrated consistently low hysteresis through various ferroelectric layer thicknesses, indicating a better capacitance matching scenario. While there remains some debate regarding which geometry is most favorable for NC-FETs [27], [28], the more stable, hysteresis-free switching observed without the interfacial metal has recently become the more preferred option.

IV. CONCLUSION

The dependence of the threshold voltage on the ferroelectric and gate dielectric thicknesses was identified, showing opposite shift when scaling the thickness of these layers.

2D NC-FETs with similar ferroelectric and dielectric thicknesses of ∼4 nm each were studied with different dielectrics, revealing Al_2O_3 to provide the most favorable interface at the scaled thickness based on switching behavior and leakage current. The lack of an interfacial metal layer in these devices resulted in suppressed ferroelectric behavior and thus less steep switching, but demonstrated consistently low hysteresis operation. Mitigating the trade-off between a more controlled gate and a more pronounced sub-60 mV/dec switching will be an important aspect of future 2D NC-FET work.

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