A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part II: Extrinsic Elements, Performance Assessment, and Design Optimization

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***Abstract*— We present a data-calibrated compact model of carbon nanotube (CNT) FETs (CNFETs), including contact resistance, direct source-to-drain, and band-to-band tunneling currents. The model captures the effects of dimensional scaling and performance degradations due to parasitic effects, and is used to study the tradeoffs between the drive current and the leakage current of CNFETs according to the selection of CNT diameter, CNT density, contact length, and gate length for a target contacted gate pitch. We describe a co-optimization study of CNFET device parameters near the limits of scaling with physical insight, and project the CNFET performance at the 5-nm technology node with an estimated contacted gate pitch of 31 nm. Based on the analysis, including parasitic resistance, capacitance, and tunneling leakage current, a CNT density of 180 CNTs/μm will enable the CNFET technology to meet the International Technology Roadmap for Semiconductors target of drive current (1.33 mA/μm), which is within reach of modern experimental capabilities.**

***Index Terms*— Carbon nanotube (CNT), carbon-nanotube FET (CNFET), compact model, contact, technology assessment, tunneling.**

I. Introduction

Semiconducting single-walled carbon-nanotube (CNT) FETs (CNFETs) have shown promise for extending the CMOS technology scaling into the sub-10-nm technology nodes [1]–[3] owing to CNTs' near-ballistic carrier transport [4], [5] and ultrathin body (1–2 nm), which provides a superior electrostatic control over the channel and enables further scaling of the gate length (L_g) below 10 nm [3], [6]. While CNFETs have superior intrinsic electronic properties, they suffer from imperfections, such as the difficulty of acquiring extremely high-purity semiconducting CNTs [7], hysteresis of the current–voltage (I–V) characteristics [8], and variations of material and devices [9]. Techniques to overcome these imperfections at the system level have been reported in [10] at modest cost of area and energy consumption.

In this paper, we focus on two specific issues: 1) parasitic metal-CNT contact resistance (R_c) and 2) direct source-to-drain tunneling (SDT) current (I_{SDT}).[1] Obtaining low R_c between metals and low-dimensional materials has been recognized as one of the most challenging yet critical requirements for high-performance transistors [11], [12]. Furthermore, as L_g scales below 10 nm, I_{SDT} may become significant and cause high leakage power [2], [13], [14]. While previous works employed rigorous yet computationally intensive modeling methods to study these issues [2], [15], here, we develop analytical models for R_c and I_{SDT} in CNFETs and study their impacts on the device performance. This paper is organized as follows: models for R_c and I_{SDT} calibrated to the experiments and numerical simulations are described in Sections II and III, respectively. These extrinsic elements are then integrated with the intrinsic model developed in [16] based on the virtual-source (VS) approach to arrive at a complete VS-CNFET model; in Section IV, the CNFET performance is evaluated at the 5-nm technology node corresponding to a contacted gate pitch $L_{\mathrm{pitch}} = 31$ nm and metal-1 pitch $L_{\mathrm{M1}} = 25.2$ nm. By comparing the drive current against the 2013 International Technology Roadmap for Semiconductors (ITRS) target [17], the requirements of the CNT density for CNFETs are presented as a guide for technology development; in Section V, we discuss the assumptions of the model and analysis as well as suggestions for future experimental works. The models presented in this paper are calibrated to the data

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[1] These two challenges are not unique to CNFETs, but are also challenges for all scaled FETs. The simplicity of the CNT band structure makes this a model system for gaining insight into these challenges for other materials as well.

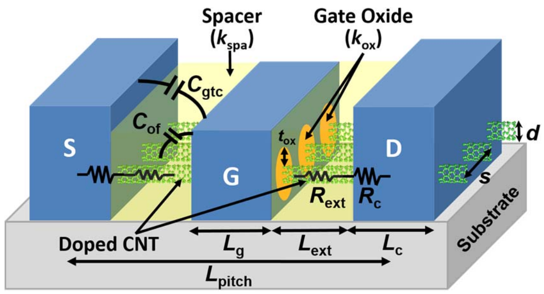

Fig. 1. Representative GAA CNFET structure used in the VS-CNFET model with the critical dimensions, parasitic resistances, and capacitances labeled.

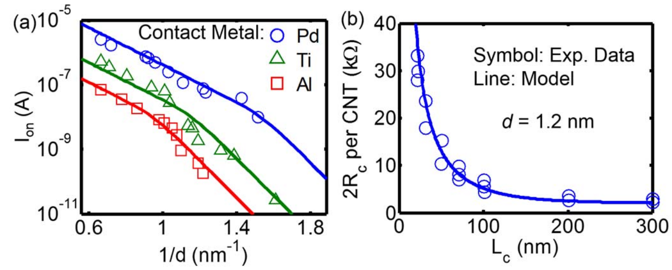

Fig. 2. Parameter extraction for the metal-CNT contact resistance model. (a) $I_{\rm ON}$ versus $1/d$ from [20] to extract E_{00} in (3a). (b) R_c versus L_c from [23] to extract λ_c and g_c in (2).

from the experiments and numerical simulations based on nonequilibrium Green's function (NEGF) quantum transport. Therefore, this paper aims to provide realistic insight into the potentials and challenges of the CNFET technology. Due to the limited space, the complete derivation of all the equations is detailed in [31]; here, we only discuss the physics and key results.

II. Parasitic Resistance

The CNFET parasitic resistance considered in this paper consists of two components: 1) the parasitic metal-CNT contact resistance (R_c) and 2) the resistance in the source/drain (S/D) extensions ($R_{\rm ext}$), as shown in Fig. 1. In general, the metal-CNT R_c is determined by three factors: 1) Schottky barrier height (ϕ_b); 2) interface quality (i.e., metal-CNT adhesion); and 3) physical contact length (L_c). In [18], the Fermi-level pinning is predicted to be insignificant in the metal-CNT contacts, and thus ϕ_b is proportional to the CNT bandgap (E_g) [19]

$$E_g = \frac{2E_p a_{\rm cc}}{d} \tag{1}$$

where $E_p = 3$ eV is the tight-binding parameter, $a_{\rm cc} = 0.142$ nm is the carbon–carbon distance in CNTs, and d is the CNT diameter. Corrections to (1) could be made due to bandgap renormalization as discussed in [16], but they do not alter the core of the model presented here. Chen *et al.* [20] experimentally demonstrated an exponential increase in R_c with $1/d$, attributed to the increase in ϕ_b; other authors showed that lower R_c can be achieved with Pd rather than Au contacts, despite their similar work functions [4], [21]. This advantage is attributed to better wettability at the Pd-CNT interface, the importance of which was also clarified by a recent study with several contact metals [22]. In the models presented here, we include the dependence of R_c on d, but not that of the interface wettability or adhesion (which could also be influenced by polymer residue from fabrication); the dependence of R_c on L_c was experimentally studied in [22] and [23], and can be phenomenologically modeled by the transmission line model [25]

$$2R_c = R_Q\sqrt{1+\frac{4}{\lambda_c g_c R_Q}}\coth\left(\frac{L_c}{L_T}\right) - R_Q \tag{2a}$$

$$L_T = \left[\frac{g_c R_Q}{\lambda_c} + \left(\frac{g_c R_Q}{2}\right)^2\right]^{-1/2} \tag{2b}$$

where L_T is the current transfer length, $R_Q = h/(4q^2) \approx 6.5$ kΩ is the quantum resistance of the CNT (lowest band, doubly degenerate with two spins), q is the elementary charge, h is Planck's constant, λ_c is the charge carrier mean-free-path (MFP) in the CNT under the metal contact, and g_c is the coupling conductance between the CNT and the metal contact. Note that in (2a), R_Q is subtracted on the right-hand side because R_Q is considered the intrinsic property associated with the interfaces between the 1-D CNT channel with the metal S/D contacts [24]. As a result, R_c is a parasitic component. In [25], λ_c and g_c are constant empirical parameters; whereas, in this paper, g_c is related to ϕ_b so as to account for the experimental observation of the increase in R_c as d decreases [20] by

$$g_c = g_{\rm co}\exp\left(-\phi_b/E_{00}\right) \tag{3a}$$

$$\phi_b = E_g/2 - (\phi_m - \phi_s) \tag{3b}$$

where ϕ_m and ϕ_s are work functions of the contact metal and the CNT, respectively, and $g_{\rm co}$ and E_{00} are empirical parameters. In analogy to the calculation of transmission coefficient through a metal-to-bulk-semiconductor Schottky contact [26], the E_{00} value in (3a) characterizes the width of the energy barrier at metal-to-bulk-semiconductor interface: 1) the smaller the E_{00} value; 2) the wider the barrier; and 3) the more sensitive the g_c value to the ϕ_b value. Note that (3b) is for p-type contacts. For n-type contacts, (3b) should be modified to $\phi_b = E_g/2 + (\phi_m - \phi_s)$.

There are three empirical parameters to be determined in (2) and (3): 1) λ_c; 2) $g_{\rm co}$; and 3) E_{00}. The extraction of these three parameters goes as follows.

1) The R_c value calculated by (2) and (3) is included into the intrinsic current model described in [16] to generate the ON-state current ($I_{\rm ON}$) compared against the data from [20] in Fig. 2(a). From the slope of $I_{\rm ON}$ versus $1/d$, $E_{00} = 32$ meV is extracted.
2) Equation (2) is fitted to the R_c versus L_c data from [23] in Fig. 2(b), where $\lambda_c = 380$ nm and $g_c = 2$ μS/nm are extracted (same as the result in [25]) for $d = 1.2$ nm with Pd as the contact metal.
3) Substituting $\phi_m = 5.1$ eV for Pd, $\phi_s = 4.7$ eV for intrinsic CNTs, $E_g = 0.71$ eV for $d = 1.2$ nm, and $g_c = 2$ μS/nm into (3a) and (3b), $g_{\rm co} = 0.49$ μS/nm is obtained. In Fig. 2(a), we observe that the $I_{\rm ON}$ drops even faster as $1/d$ increases beyond a certain point

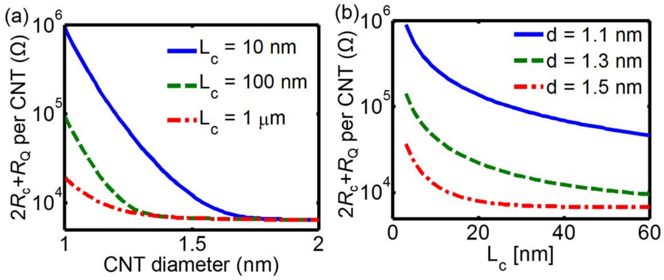

Fig. 3. Contact resistance versus (a) CNT diameter for different contact lengths and (b) contact lengths for different CNT diameters.

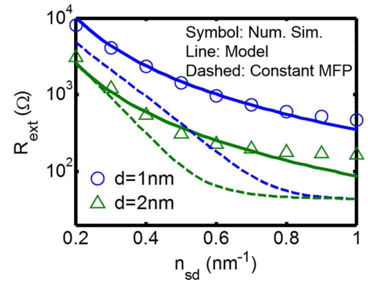

Fig. 4. Comparison of the extension resistances versus the doping density. The symbols are calculated by (4) numerically. Lines: analytical approximation of (5). The dashed lines are generated by assuming λ_i in (4) is constant.

(for the Al contact as example, the I_{ON} decreases more rapidly as $1/d > 1\ \mathrm{nm}^{-1}$).

This accelerated downturn can be explained as follows: when $1/d$ is small and g_c is large, $L_T \ll L_c$ in (2) and $\coth(L_c/L_T) \approx 1$. Therefore, R_c increases with $(1/g_c)^{1/2} \propto \exp[1/(2d)]$; as $1/d$ increases and g_c becomes small, $L_T \gg L_c$ and $\coth(L_c/L_T) \approx L_T/L_c$, and R_c increases with $1/g_c \propto \exp(1/d)$. This accelerated downturn is observed in both the experimental data and the model (2) and (3), which strengthens the validity of the R_c model. As shown in Fig. 3, in the region where L_c and/or d are small, R_c increases drastically, which severely degrades the drive current and can cause large variation in the presence of variations in L_c and d. The impact of L_c and d on the CNFET performance is discussed in Section IV.

The other component R_{ext} is derived from the 1-D Landauer formula [24]

$$R_{\mathrm{ext}} = 1/G - R_Q \tag{4a}$$

$$G = \frac{4q^2}{h}\int_{E_c}^{\infty}\frac{\lambda_i(E)}{L_{\mathrm{ext}}+\lambda_i(E)}\left[-\frac{\partial f(E,E_F)}{\partial E}\right]dE \tag{4b}$$

$$n_{\mathrm{sd}} = \int_{E_c}^{\infty} g(E) f(E,E_F)\,dE \tag{4c}$$

where G is the CNT conductance at low fields, L_{ext} is the length of the S/D extensions (see Fig. 1), E_c is the conduction band (CB) edge, E_F is the Fermi level, E is the energy of free electrons referenced to E_c, f is the Fermi–Dirac distribution function, $g(E)$ is the CNT density of states, n_{sd} is the doping density in the S/D extensions, and λ_i is the carrier MFP in CNTs representing the aggregate effect of optical phonon and acoustic phonon scattering as introduced in [27]. R_Q is subtracted from $1/G$ in (4a) because G is the total conductance including the contact resistance, which has already been considered in the R_c model. Because λ_i has a complex expression [27], (4b) cannot be integrated analytically. Therefore, an empirical expression of R_{ext} is employed here

$$R_{\mathrm{ext}} = R_{\mathrm{ext0}}\frac{L_{\mathrm{ext}}}{d^{\alpha_d} n_{\mathrm{sd}}^{\alpha_n}} \tag{5}$$

where R_{ext0}, α_d, and α_n are the empirical fitting parameters. The form of (5) is inspired by the observations that: 1) for heavily doped CNTs, the carrier transport becomes more diffusive, and thus $R_{\mathrm{ext}} \propto L_{\mathrm{ext}}/n_{\mathrm{sd}}$ in a manner analogous to the Drude model and 2) λ_i is proportional to d according to [27]. Equation (5) is then fitted to the numerical results given by (4), as shown in Fig. 4, where $R_{\mathrm{ext0}} = 35\ \Omega$, $\alpha_d = 2$, and $\alpha_n = 2.1$ are extracted. Equation (5) agrees well with (4) at low n_{sd} region but underestimates R_{ext} at high n_{sd} region. However, when n_{sd} is large, $R_{\mathrm{ext}} \ll R_c$, so the discrepancy is negligible. The dashed lines in Fig. 4 represent the results when λ_i is a constant instead of being dependent on energy and CNT diameter. In such a case, R_{ext} exhibits less sensitivity to d and higher sensitivity to n_{sd}.

III. Tunneling Leakage Current

According to the 2013 ITRS projections [17], the L_g values of MOSFETs should eventually scale below 10 nm. At such a small L_g, quantum mechanical tunneling from the source to drain becomes appreciable. Several simulation works predicted that at $L_g \approx$ 5–10 nm, I_{SDT} will become prominent and severely degrade the subthreshold swing (SS) of MOSFETs [2], [13], [14]. Nonetheless, observation of SDT has been reported only in a few experiments, e.g., a Si MOSFET with $L_g = 8$ nm, using temperature-dependent measurements [28]. Whether the ultimate scaling limit of L_g is set by I_{SDT} is still not clear because of the lack of experimental evidence, and because the answer also depends on the precise geometry of the FET. However, to fully exploit the excellent electrostatic control of the ultrathin CNTs, the L_g value of CNFETs is likely to be aggressively scaled down until the leakage current becomes intolerable. It is thus important to develop a model that consider the impact of I_{SDT} in the sub-10-nm technology nodes.

Two tunneling mechanisms are considered here: 1) SDT and 2) band-to-band tunneling (BTBT) at the drain side. The SDT can be further divided into two parts: 1) the intraband SDT (intra-SDT), the tunneling from CB to CB, and 2) the inter-band SDT (inter-SDT), the tunneling from CB to valence band (VB) to CB. The BTBT is the tunneling from source VB to drain CB, as shown in Fig. 5. While n-type FETs are used as examples throughout this paper, the model can be easily applied to p-FETs by properly changing the polarity of the terminal voltages, due to the symmetry of the CNT CB and VB. All tunneling currents are computed by the 1-D Landauer formula [24]

$$I = \frac{4q}{h}\int T_e(E)[f(E,E_{\mathrm{fs}}) - f(E,E_{\mathrm{fd}})]\,dE \tag{6}$$

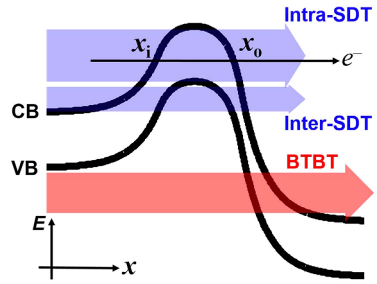

Fig. 5. Illustration of the direct SDT and the BTBT mechanisms. x_i and x_o are the positions where the electrons tunnel in and out the energy barrier.

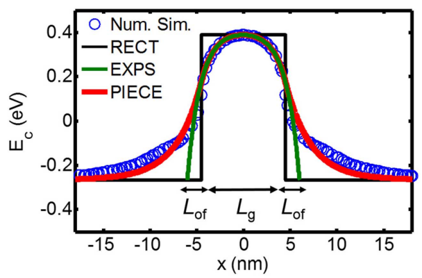

Fig. 6. CB profile calculated by the numerical simulation (circles) [30]. The three analytical models. RECT: rectangular E_c profile. EXPS: two connected exponential functions given by (9). PIECE: piecewise function given by (10).

where T_e is the tunneling probability and E_{fs} and E_{fd} are Fermi levels at the source and the drain, respectively. T_e is calculated by the Wentzel–Kramers–Brillouin approximation [29]

$$T_e(E) = \exp\left(-2\int_{x_i}^{x_o} \kappa dx\right)$$
$$\kappa = \frac{\pi E_g}{h v_F}\sqrt{1 - \{1 - 2[E_c(x) - E]/E_g\}^2} \quad (7)$$

where κ is the imaginary wave vector in CNTs, $v_F \approx 10^6$ m/s is the Fermi velocity, x is the position along the CNFET channel, and x_i and x_o are the positions where the electrons tunnel in and out the energy barrier, respectively (see Fig. 5). Equation (7) is then recast as follows for the convenience of calculations:

$$T_e(E) = \exp\left[-\frac{2\pi E_g}{h v_F} t_b(E)\right]$$
$$t_b(E) = \int_{x_i}^{x_o} \sqrt{1 - \{1 - 2[E_c(x) - E]/E_g\}^2} dx. \quad (8)$$

To calculate T_e, analytical models for $E_c(x)$ are first discussed.

The circles in Fig. 6 are the E_c profile calculated by the numerical simulation based on the NEGF quantum transport [30], which simulates a CNFET with a cylindrical gate-all-around (GAA) device structure and heavily doped S/D extensions. Two features are observed in the simulated E_c profile: 1) a curvy profile around the top of $E_c(x)$ and 2) gradual tails extending into the S/D extensions. Three different analytical models of $E_c(x)$ are examined here: 1) a rectangular profile (named RECT in Fig. 6); 2) two connected exponential functions to model the curvy top of $E_c(x)$ (named EXPS in Fig. 6)

$$E_c(x) = \begin{cases} E_{cs}(x) = u_s e^{-x/\lambda} + v_s, & -L_g/2 - L_{of} < x < 0 \\ E_{cd}(x) = u_d e^{x/\lambda} + v_d, & 0 < x < L_g/2 + L_{of} \end{cases} \quad (9)$$

where u's and v's are fitting coefficients, λ is the electrostatic length scale discussed in [16], and L_{of} is an empirical parameter functioning like an extension of the L_g that captures the finite Debye length and the gate fringing field (see Fig. 6); and 3) a piecewise function to describe both the curvy top and the tails of $E_c(x)$ (named PIECE in Fig. 6)

$$E_c(x) = \begin{cases} E_{cs}(x) = b_s e^{(x+L_g/2)/\lambda_s} + c_s, & x < -L_g/2 \\ E_{cg}(x) = a_1 e^{-x/\lambda} + a_2 e^{x/\lambda} + a_3 \\ \qquad\qquad -L_g/2 < x < L_g/2 \\ E_{cd}(x) = b_d e^{-(x-L_g/2)/\lambda_d} + c_d, & x > L_g/2 \end{cases} \quad (10)$$

where a's, b's, c's, λ_s, and λ_d are fitting coefficients. By substituting (9) and (10) into (8), T_e can be calculated analytically. The derivation of the coefficients in (9) and (10) as well as the analytical expressions of T_e in (8) are detailed in [31, eq. (28)–(36)]. I_{SDT} is then calculated by (6) numerically.

I_{SDT} calculated by the numerical simulation [30] is compared against the three different $E_c(x)$ models individually in Fig. 7(a)–(c). As shown in Fig. 7(a), the RECT model does not fit the data well in the high V_{gs} region (i.e., near-threshold), because it fails to capture the characteristic of the curvy top of E_c, resulting in an underestimate of I_{SDT}; in the low V_{gs} region (i.e., deep subthreshold region), the RECT model overestimates I_{SDT} due to the disregard of the tails of the E_c profile; in Fig. 7(b), the EXPS model fits the data well at high V_{gs} but overestimates I_{SDT} at low V_{gs} because it also fails to capture the tails; finally, in Fig. 7(c), the PIECE model gives the best fitting result because it considers both the curvy top and the tails. However, the use of a piecewise function in (10) could potentially result in convergence issues when implemented in Verilog-A [32], because when a large-scale circuit is simulated in an environment like SPICE, extraordinarily large biases may be applied on the device terminals, which can potentially lead to discontinuities in (10). As a result, the EXPS model will be used to calculate I_{SDT} in the following analysis. Although the EXPS model overestimates I_{SDT} in the deep subthreshold region, it can still give accurate results in the subthreshold region and warn the user of an imminent significant impact of I_{SDT} when the L_g becomes too short. Besides, the EXPS model is more computationally efficient.

As shown in [33], the presence of I_{SDT} significantly degrades the SS and increases the leakage power of CNFETs. To explore potential ways to lower I_{SDT}, Fig. 8(a) and (b) shows how I_{SDT} is affected by d, n_{sd}, and the dielectric constant of the sidewall spacer k_{spa} (see Fig. 1). As shown in Fig. 8(a), I_{SDT} increases exponentially with d, because κ in (7) is proportional to E_g. By utilizing small-diameter CNTs, tunneling leakage can be effectively mitigated, but it also leads to lower drive current due to larger R_c, and lower carrier mobility and velocity [16]. A decrease of n_{sd} from 1 nm^{-1} to 0.6 nm^{-1} can reduce I_{SDT} by a factor of 3.5,

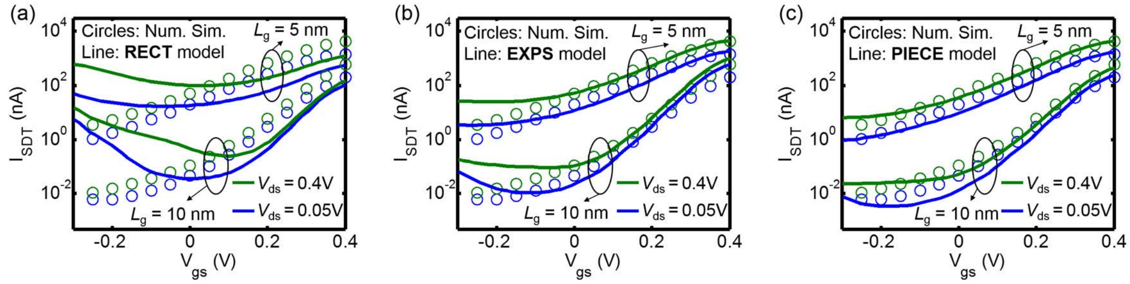

Fig. 7. Comparison of direct source-to-drain tunneling current between the numerical simulation [30] and the three models. (a) RECT: rectangular E_c profile. (b) EXPS: E_c profile given by (9). (c) PIECE: E_c profile given by (10) for different gate lengths. $d = 1$ nm is used.

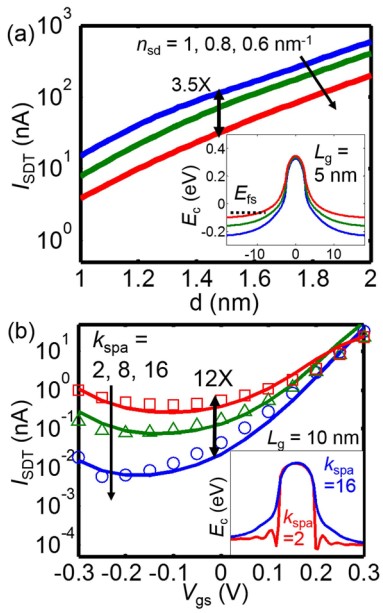

Fig. 8. (a) Direct SDT current I_{SDT} versus CNT diameters for different doping densities in the S/D extensions. Inset: source CB is raised as n_{sd} decreases. (b) I_{SDT} versus V_{gs} for different spacer dielectric constants (k_{spa}). Symbol: numerical simulation. Line: model. Inset: higher k_{spa} results in stronger gate-to-extension fringe field, wider energy barrier, and lower I_{SDT}.

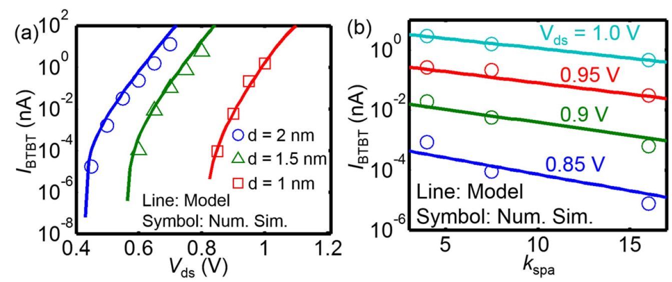

Fig. 9. Calibration of the BTBT current model to the numerical simulation [30] for different CNT diameters and spacer dielectric constants k_{spa}. (a) I_{BTBT} versus V_{ds} for different diameters. (b) I_{BTBT} versus k_{spa} for different values of V_{ds}s.

because as n_{sd} decreases, the CB edge at the source is raised relative to the Fermi level, and thus less carriers are available to tunnel from the source through the barrier to the drain [see Fig. 8(a) (inset)]. However, lower n_{sd} gives higher R_{ext}. As shown in the inset of Fig. 8(b), higher k_{spa} results in stronger gate-to-extension fringe field and leads to a wider energy barrier. To model the effect of the fringe field caused by different k_{spa}'s, L_{of} in (9) and implicitly in (10) are empirically related to k_{spa} and the gate oxide thickness t_{ox}

$$L_{\mathrm{of}} = (0.0263k_{\mathrm{spa}} + 0.056) \cdot t_{\mathrm{ox}}. \tag{11}$$

As shown in Fig. 8(b), increasing k_{spa} from 2 to 16 can reduce I_{SDT} by a factor of 12 for $L_g = 10$ nm and $d = 1$ nm. However, increasing k_{spa} also causes larger parasitic capacitances and degrades the circuit speed [34]. These results indicate that lowering I_{SDT} may degrade the speed performance (i.e., increase delay), a manifestation of the energy-delay tradeoffs. Note that (11) is a first-order approximation, and the empirical coefficients are determined by fitting the I_{SDT} model to the numerical simulation based on a GAA cylindrical structure [30] for different values of k_{spa} and t_{ox}. While (11) could be changed for different device geometries, the trend should remain the same.

The BTBT current (I_{BTBT}) is modeled in a similar approach to I_{SDT}, except that the E_c value is modeled differently

$$E_c(x) = ue^{-x/\lambda_{\mathrm{BTBT}}} \tag{12}$$

where u and λ_{BTBT} are fitting parameters. Equation (12) is employed to model the decaying E_c profile at the gate-drain junction (see Fig. 5). Substituting (12) into (8) gives

$$t_b(E) = \int_{x_i}^{x_o} \sqrt{1 - \{1 - 2(ue^{-x/\lambda_{\mathrm{BTBT}}} - E)/E_g\}^2}dx$$
$$x_i = \lambda_{\mathrm{BTBT}} \ln\left(\frac{E + E_g}{u}\right), \quad x_o = \lambda_{\mathrm{BTBT}} \ln\left(\frac{E}{u}\right). \tag{13}$$

By changing variables, a closed-form expression of t_b is obtained

$$t_b = \lambda_{\mathrm{BTBT}}\pi(\zeta + \sqrt{\zeta^2 - 1}) \tag{14}$$

where $\zeta = -2E/E_g - 1$ (see [31] for detailed derivation). I_{BTBT} is then obtained by integrating (6) numerically. The modeled I_{BTBT} is compared against the numerical simulation in Fig. 9(a) and (b). Similar to the discussion of the effect of gate-to-drain fringe fields when modeling I_{SDT}, I_{BTBT} is also a function of k_{spa}. The higher the k_{spa} value, the stronger the fringe fields, the more gradual the E_c profile at the gate-drain junction, and the smaller the I_{BTBT} value. Empirically, λ_{BTBT} (nm) $= 0.092k_{\mathrm{spa}} + 2.13$ is determined by fitting the I_{BTBT} model to the numerical simulation result.

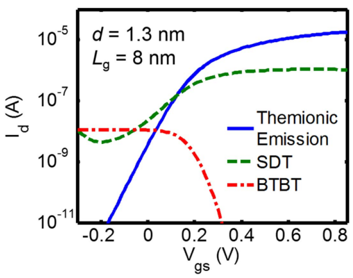

Fig. 10. Representative I_d versus V_{gs} of a CNFET with $L_g = 8$ nm and $d = 1.3$ nm, showing that the tunneling currents dominate over the thermionic emission current in the subthreshold region.

Note that phonon-assisted and trap-assisted tunneling [35] are not considered in this model, so $I_{\text{BTBT}} = 0$ when $V_{\text{ds}} < E_g$. In addition, since the tunneling model presented in this paper is calibrated to the NEGF-based numerical simulation with a relatively simple GAA cylindrical device structure [30] assuming ballistic transport, the model aims to provide a trend instead of accurate results.

IV. CNFET Performance Assessment

The intrinsic elements of the VS-CNFET model introduced in [16] are then combined with the extrinsic elements described in Sections II and III to assess the CNFET design space and performance. A representative I_d versus V_{gs} curve given by the complete VS-CNFET model separately identifying the current components—thermionic emission, direct SDT, and BTBT currents—is shown in Fig. 10. It can be seen that the tunneling currents can dominate over the thermionic emission current in the subthreshold region of a short-channel CNFET.

In this section, we demonstrate the capability of the VS-CNFET model by optimizing L_g, L_c, L_{ext}, and CNT diameter to minimize the CNFET gate delay (τ_{gate}) and estimating the requirement for CNT density ($\rho_{\text{cnt}} \equiv 1/s$, where s is the spacing between CNTs, see Fig. 1) to meet the ITRS targets of drive current. For advanced CMOS technology, the dimensional scaling is no longer simply the scaling of L_g but a multivariable optimization that targets a technology pacing objective. Fig. 11 shows the dimensional scaling trend of major foundries as well as the projections down to the so-called 5-nm technology node by linear extrapolation. While foundries tend to scale the metal-1 pitch (L_{M1}) and the contacted gate pitch (L_{pitch}, as shown in Fig. 1) at different paces, the geometric pitch $L_{\text{GP}} \equiv (L_{\text{M1}} \cdot L_{\text{pitch}})^{1/2}$ scales at a relatively consistent pace. Here, we use this L_{GP} to pace the advancement of logic technology. The CNFET performance is evaluated at the 5-nm node corresponding to $L_{\text{GP}} = 28.1$ nm, $L_{\text{M1}} = 25.2$ nm, and $L_{\text{pitch}} = 31.1$ nm. The 2023 node of the 2013 ITRS projections [17] is used as a reference point, which also predicts L_{M1} will be scaled down to 25.2 nm in 2023 for high-performance logic. The corresponding ITRS parameters—supply voltage $V_{\text{dd}} = 0.71$ V and EOT $= 0.51$ nm—are used as the inputs to the VS-CNFET model. Furthermore, a GAA device structure is assumed (see Fig. 1) in the following analysis.

Under the constraint of a fixed L_{pitch}, tradeoffs exist between L_g, L_c, and L_{ext} at the device-level. Scaling down L_g helps to improve the device speed because of lower intrinsic capacitance and higher drive current, but also increases the OFF-state current (I_{OFF}, defined as the I_d at $V_{\text{gs}} = 0$ and $V_{\text{ds}} = V_{\text{dd}}$) and thus the static power. Hence, there exists an optimal L_g to balance the speed and power consumption. L_c is preferred to be as long as possible in order to lower the R_c value (ignoring the possible increase in the parasitic capacitance at the circuit level). Scaling down L_{ext} helps to reduce R_{ext} but drastically increase the parasitic capacitance (C_{par}). For CNFETs, R_{ext} is negligible compared with R_c in general, so L_{ext} is preferred to be large.

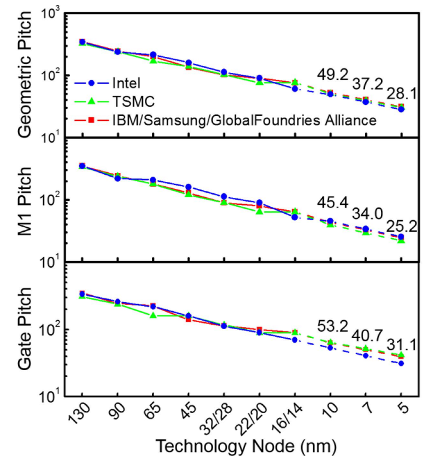

Fig. 11. Dimensional scaling trend of major foundries collected from the published data (unit in nm). The geometric pitch is defined as (metal-1 pitch $\times$ contacted gate pitch)$^{1/2}$. The dashed lines beyond the 16/14-nm node are projections by linearly extrapolation from the nodes over the last 10 years.

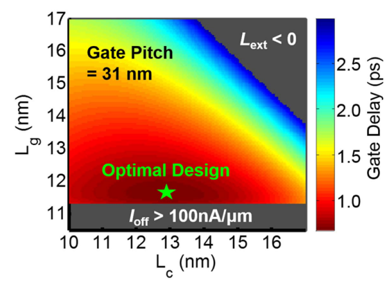

Fig. 12. Optimization of the CNFET dimensions (L_g, L_c, and L_{ext}) to minimize the gate delay under the constraints of $L_{\text{pitch}} = 31$ nm and $I_{\text{OFF}} = 100$ nA/μm. $\rho_{\text{cnt}} = 100$ CNTs/μm and $d = 1.2$ nm are used.

In Fig. 12, L_g, L_c, and L_{ext} are optimized under the constraints of $L_{\text{pitch}} = 31$ nm and $I_{\text{OFF}} = 100$ nA/μm (by adjusting the flat-band voltage V_{fb}) to minimize $\tau_{\text{gate}} \equiv (L_g C_{\text{inv}} + C_{\text{par}}) \cdot V_{\text{dd}}/I_{\text{ON}}$, where C_{par} is calculated by the analytical models of [36], in which the gate-to-extension fringe capacitance (C_{of}) and gate-to-contact capacitances (C_{gtc}) are considered (see Fig. 1). $\rho_{\text{cnt}} = 100$ CNTs/μm is assumed. The optimal design is arrived at $L_g = 11.7$ nm, $L_c = 12.9$ nm, and $L_{\text{ext}} = 3.2$ nm. Because the optimization goal is to minimize τ_{gate} and R_c is the major limiter of the drive current, L_g is scaled down until I_{OFF} becomes intolerable, and L_{ext} is scaled down until C_{par} becomes too large, in order to save space for L_c. It is worthwhile noting that while the optimal design

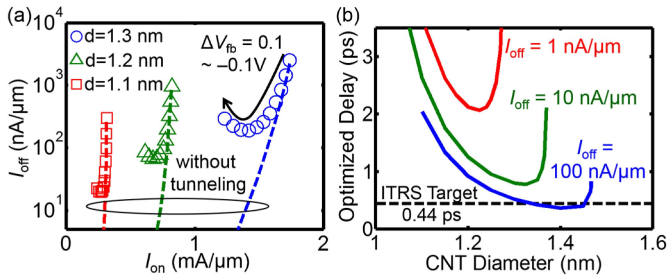

Fig. 13. (a) I_{ON} versus I_{OFF} for different diameters. The symbols are generated by sweeping ΔV_{fb} from -0.1 to 0.1 V. CNTs with smaller d have smaller I_{ON} mainly due to larger R_c. (b) Optimized gate delay (see Fig. 12) versus diameter under different constraints of I_{OFF}. $\rho_{\mathrm{cnt}} = 100$ CNTs/μm is assumed.

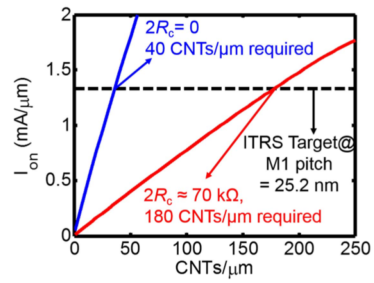

Fig. 14. Projection of the requirement for the CNT density to meet the 2013 ITRS target of $I_{\mathrm{ON}} = 1.33$ mA/μm with fixed $I_{\mathrm{OFF}} = 100$ nA/μm corresponding to metal-1 pitch $= 25.2$ nm. $2R_c \approx 70$ kΩ per CNT is calculated by (2) with $L_c = 12.9$ nm and $d = 1.2$ nm.

may vary as different parameters (e.g., CNT diameter) are used, the shape of the contour in Fig. 12 remains the same.

It appears in Fig. 12 here that L_g cannot scale below 11 nm in order to keep $I_{\mathrm{OFF}} \leq 100$ nA/μm, mainly due to SDT. Since SDT highly depends on the CNT diameter, the impact of the CNT diameter is studied in Fig. 13. Fig. 13(a) shows I_{ON} versus I_{OFF} for different diameters. A minimum I_{OFF} for each d is observed by sweeping V_{fb}: as V_{fb} starts increasing, I_{OFF} decreases exponentially because both thermionic emission and intra-SDT currents decrease; as V_{fb} further increases beyond a certain point, inter-SDT starts to increase and becomes dominant, so I_{OFF} increases. The larger the diameter, the higher the I_{OFF} value. In addition, for small-diameter CNTs, reducing V_{fb} does not improve I_{ON} effectively, because the R_c value is so large that the I_{ON} value is dominated by the resistance of contacts rather than the channel. In Fig. 13(b), we co-optimize the CNT diameter, L_g, L_c, and L_{ext} to minimize τ_{gate} under different constraints of I_{OFF}. Each point along the curves has different optimized L_g, L_c, and L_{ext}. The optimal diameter increases as the constraint of I_{OFF} increases, indicating that large-diameter CNTs are suitable for high-performance applications while small-diameter CNTs are suitable for low-power applications.

In the discussion above, the CNTs are assumed to be perfectly aligned and equally spaced, and $\rho_{\mathrm{cnt}} = 100$ CNTs/μm is assumed. This CNT density is within reach experimentally as suggested in recent reports. The highest ρ_{cnt} to date through chemical vapor deposition is $\approx$30 CNTs/μm [37]. By using multiple CNT transfers, $\rho_{\mathrm{cnt}} \approx 100$ CNTs/μm was achieved [38]. Although $\rho_{\mathrm{cnt}} > 500$ CNTs/μm has been reported in [39] by assembling solution-based CNTs using the Langmuir–Schaefer method on a target substrate, the CNTs were not well aligned and the measured $R_c \approx 3$ MΩ/CNT, about 100$\times$ the value reported in [23]. While high ρ_{cnt} has been reported in these works, the control of CNT pitch still remains to be a challenge. Variations in the CNT pitch can degrade CNFET performance and reduce circuit yield. The issue of CNT variations has been discussed in [10], and is out of the scope of this paper.

To estimate the ρ_{cnt} required for CNFETs to deliver enough drive current (assuming no variations), Fig. 14 shows I_{ON} versus ρ_{cnt} with a fixed $I_{\mathrm{OFF}} = 100$ nA/μm; $d = 1.2$ nm is used for the analysis, because it is the diameter measured in the experiments that the model is calibrated to [16]; $L_g = 11.7$ nm and $L_c = 12.9$ nm are used according to the optimization result from Fig. 12. At $L_c = 12.9$ nm, $2R_c \approx 70$ kΩ per CNT, and $\rho_{\mathrm{cnt}} \approx 180$ CNTs/μm is needed in order to meet the 2013 ITRS target of $I_{\mathrm{ON}} = 1.33$ mA/μm (corresponding to $L_{\mathrm{M1}} = 25.2$ nm); whereas when R_c can be reduced to zero, the required ρ_{cnt} can be lowered to 40 CNTs/μm.

V. Discussion

The analysis in Section IV exhibits the potential of scalability of CNFETs down to $L_{\mathrm{pitch}} = 31$ nm and capability of delivering high drive current with ON/OFF ratio $>10^4$. It is important to review the assumptions made in the analysis. The interface between the gate dielectric and the CNTs is assumed to be perfect, i.e., hysteresis of the I–V characteristics [8] is negligible, and the short-channel effect (e.g., SS degradation and Drain-Induced Barrier Lowering) is determined purely by electrostatics. Recent progress in the CNT-dielectric interface includes the use of Y_2O_3 and LaO_3 as gate dielectrics to reduce the interface traps [40], [41] and interface passivation to alleviate the hysteresis [8], [42]. The CNTs are assumed to be perfectly aligned and equally spaced. The imperfect alignment and variation in the CNT spacing result in delay variations and potential functional failures. Process techniques to achieve a good CNT alignment have been improved over the years [43]. Design techniques can be employed to overcome these imperfections at the modest cost of area and energy consumption [10]. Nonetheless, improvement in the material is still strongly desired. The CNTs in a single device are assumed to be identical in diameter, carrier mobility, and velocity. However, Cao *et al.* [9] measured the distribution of CNT diameter and mobility, showing that the variations are not negligible. As these imperfections are considered, the projections described in Section IV need to be adjusted, but the general conclusion should remain unchanged (e.g., tradeoff between contact resistance and tunneling currents due to the selection of CNT diameter).

Since the CNT diameter is shown to have a great impact on R_c, I_{SDT}, and thus the CNFET performance, we next revisit the model and discuss its validity. The dependence of R_c on d is characterized in (3) by E_{00}, which can be viewed (loosely) as the inverse of the Schottky barrier width at the metal-CNT contacts. Smaller E_{00} leads to higher sensitivity of R_c to the CNT diameter. In this paper, $E_{00} = 32$ meV is extracted from [20]. However, the detailed experimental studies on the dependence of R_c on d are still lacking, and whether small-diameter CNTs will lead to such a large R_c (see Fig. 3) that the drive current of CNFETs becomes too small for practical applications needs to be verified by more careful investigation. On the other hand, though large-diameter CNTs can give lower R_c, it also causes high tunneling leakage current. As shown in Fig. 8, I_{SDT} increases drastically as d increases. The model of tunneling currents developed in Section III is calibrated to the numerical simulation [30]. However, to date, only a few experimental works have observed I_{SDT} in the Si-MOSFET with $L_g = 8$ nm [28], and the experimental observation of I_{SDT} in CNFETs has not been reported yet. For a CNFET with $L_g = 9$ nm and $d \approx 1.3$ nm, as reported in [3], I_{SDT} is expected to be appreciable, but has not yet been clearly observed. One manifestation of I_{SDT} is the degradation of SS. Temperature-dependent measurement of SS can be helpful to identify the existence of I_{SDT}: if I_{SDT} is not prominent, the SS will decrease as the temperature goes down; and if I_{SDT} is significant, the SS will not decrease but remain relatively unchanged as the temperature goes down, as described in [28]. Since large-diameter CNTs can provide higher drive current, research on whether the tunneling current in scaled CNFETs is tolerable or not is of crucial importance, and the temperature-dependent measurement is suggested to be an effective means to identify the existence of I_{SDT}.

VI. Conclusion

We present data-calibrated analytical models for the metal-CNT contact resistance, direct SDT, and BTBT leakage currents in CNFETs, which are integrated with the intrinsic model elements to arrive at a complete CNFET model for performance assessment. We predict that a density of 180 CNTs/μm is required to meet the ITRS targets of OFF-state and ON-state currents at the 5-nm technology node corresponding to 25.2-nm metal-1 pitch and 31-nm contacted gate pitch assuming no variations; in contrast, a density of 40 CNTs/μm would be enough if the parasitic contact resistance can be eliminated. The experimental demonstrations of >100 CNTs/μm are available today [38], but whether these are sufficient for highly scaled CNFETs remains to be seen, depending on R_c optimization and diameter selection, as discussed in this paper. The in-depth study of R_c and its dependence on d is highly desirable in order to identify further device design points for the CNFET technology in the sub-10-nm nodes.

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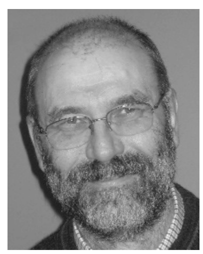

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