A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-nm Regime—Part I: Intrinsic Elements

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***Abstract*— We present a data-calibrated compact model of carbon nanotube (CNT) FETs (CNTFETs) based on the virtual-source (VS) approach, describing the intrinsic current–voltage and charge–voltage characteristics. The features of the model include: 1) carrier VS velocity extracted from experimental devices with gate lengths down to 15 nm; 2) carrier effective mobility and velocity depending on the CNT diameter; 3) short channel effect such as inverse subthreshold slope degradation and drain-induced barrier lowering depending on the device dimensions; and 4) small-signal capacitances including the CNT quantum capacitance effect to account for the decreasing gate capacitance at high gate bias. The CNTFET model captures the dimensional scaling effects and is suitable for technology benchmarking and performance projection at the sub-10-nm technology nodes.**

***Index Terms*— Carbon nanotube (CNT), CNTFET, compact model, technology assessment.**

I. Introduction

CARBON nanotube (CNT) FETs (CNTFETs) based on single-walled semiconducting CNTs have been among the foremost candidates to complement Si and extend CMOS technology scaling in the sub-10-nm technology nodes [1]–[3]. One of the dominant factors impeding further scaling of Si MOSFETs is the short-channel effect (SCE), which causes FETs at short gate lengths to be difficult to turn OFF, consequently consuming too much power [4]. Further scaling the gate length (L_g) of Si-MOSFETs requires an ultrathin channel body, resulting in low drive current due to mobility degradation (caused by the body thickness fluctuation [5]) and low density of states (DOS) [6].

By contrast to bulk 3-D materials, a single-walled CNT is essentially a single sheet of graphene rolled into a seamless cylinder with a 1–2 nm diameter. Because of the atomically thin body, the gate control of the CNTFETs is superior and the SCE can be overcome even for $L_g < 10$ nm [3], [7], [8]. Furthermore, the CNTs show promise for energy-efficient computation because of their high carrier velocity and near-ballistic carrier transport property [9], [10]. Recent progress and challenges in the CNTFET technology can be found in [1]–[3] and [11]–[15].

For all emerging technologies, early assessment based on both experimental observation and theoretical study is of great value as it facilitates identification of the most promising options and allows resources to be focused on them. Nonequilibrium Green's function (NEGF) formalism [16] has been extensively employed to simulate the quantum transport in CNTFETs and assess their performance [7], [8], [17]. However, the NEGF is too computationally expensive for performance assessment at the application level. Compact modeling based on the Landauer formula for ballistic transport in the CNTs is another efficient approach for performance assessment [18]–[20]. However, the effects of dimensional scaling, series resistance (R_s), and tunneling leakage current have not been well captured in these compact models. Attempts were made to address these issues by lumping the scaling and parasitic effects into constant input parameters [e.g., constant R_s and subthreshold slope (SS)] independent of the device design [18]. As a result, the dimensional scaling effect and variations cannot be studied.

In this paper, we describe a data-calibrated compact CNTFET model based on the virtual-source (VS) approach [21]. This VS-CNTFET model captures device parasiticand dimensional scaling effects, and has been implemented in Verilog-A [22] available online [23]. The motivation of developing the model is twofold.

1) Assess the performance of CNTFET and study the design tradeoffs, including device parasitic and process variations, at the extremely scaled dimensions.
2) Identify the required improvement in the current CNTFET technology to achieve performance advantage over similarly scaled FETs.

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In the VS-CNTFET model, the VS parameters described in Section II are connected to the CNTFET dimensions and the CNT diameter to capture the scaling effect. A similar concept has been reported in [24], but it did not include several important effects: 1) small-signal capacitances were not properly modeled; 2) the CNT quantum capacitance was not considered; 3) the internal VS parameters were independent of the CNT diameter; and 4) iterations and numerical integral were needed. These deficiencies are addressed in this two-part paper.

Several premises are relied on in this paper.

1) We focus purely on the MOSFET-like CNTFETs with Ohmic metal-CNT contacts, because they provide better performance and could be realized by heavily doping the source/drain (S/D) extensions [25]. Previous efforts on modeling the Schottky-barrier CNTFETs can be found in [26].
2) The n-type CNTFETs are discussed throughout this paper. Although the CNTFETs in ambient air are usually p-type based on the preferred injection of holes at the contacts, the n-type CNTFETs have been achieved by contact or interface engineering [27], [28], and from a physical and mathematical point of view the operation of n-type and p-type CNTFETs is symmetric due to the symmetry of conduction and valence bands.
3) Only the first subband in CNTs is considered because most digital applications call for a low-power supply voltage, but higher subbands can be easily included with proper modification of the charge model.

This paper is organized as follows. Analytical expressions that connect the VS parameters to the CNTFET design as well as the model calibration are described in Section II. The charge model used to derive the small-signal capacitances is introduced in Section III. In Section IV, the impact of CNT diameter on the intrinsic CNTFET performance is presented. Finally, in Section V, the issues pertaining to the VS parameter extraction from the CNTFETs are discussed. Due to the limited space, the complete derivation of all the equations is detailed in [23]; here, we only discuss the physics and key results. Models for the contact resistance and tunneling leakage current, and demonstration of the use of the model will be introduced in Part II of this two-part paper [29].

II. Virtual Source Model for CNTFETs

The VS model is a semiempirical model with only a few physical parameters, originally developed for short-channel Si MOSFETs that have a gate-controlled source-injection barrier [21], [30]. Based on the VS approach, the drain current (I_d) of a MOSFET is the product of the mobile charge density and the carrier velocity at the VS, defined as the top of the energy barrier near the source in the ON-state. There are ten VS parameters: 1) gate length (L_g); 2) gate capacitance in strong inversion region ($C_{\rm inv}$); 3) low-field effective mobility (μ); 4) threshold voltage (V_t); 5) inverse SS factor ($n_{\rm ss}$); 6) drain-induced barrier lowering (DIBL) coefficient (δ); 7) series resistance (R_s); 8) VS carrier velocity ($v_{\rm xo}$); 9) fitting parameter α; and 10) fitting parameter β used to smooth the transitions between weak and strong inversion, and between nonsaturation and saturation regions, respectively. In this section, the VS parameters are associated with the device dimensions and CNT diameter (d), which is a crucial parameter because it determines the CNT band structure and the bandgap (E_g). In this paper, the CNT $E_g = 2E_p a_{\rm cc}/d$ is derived from the Hückel tight-binding model [31], where $E_p = 3$ eV is the tight-binding parameter and $a_{\rm cc} = 0.142$ nm is the carbon–carbon distance in the CNTs, indicating $E_g \approx 0.85/d$ eV with d in nanometer. Corrections to the model of E_g could be made due to bandgap renormalization induced by many-body interaction [32] or substrate-induced polarization effects [33], but they do not alter the essence of the VS model presented here.

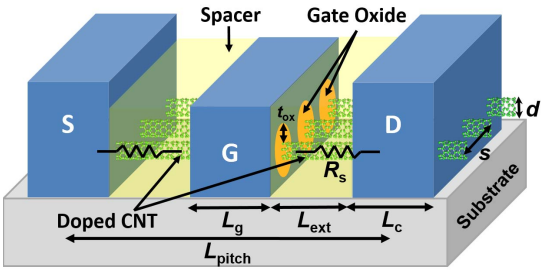

Fig. 1. Representative gate-all-around CNTFET device structure used in the VS-CNTFET model with the critical dimensions labeled.

A representative Gate-All-Around (GAA)-CNTFET device structure used in the VS-CNTFET model is shown in Fig. 1 with the critical dimensions labeled. By calibrating the VS-CNTFET model to the experimental data and rigorous numerical simulations, it becomes possible to make predictive estimates of device behavior as the dimensions scale down. Although the VS model was not originally meant to be predictive because the VS parameters need to be extracted from the current–voltage (I–V) and capacitance–voltage (C–V) measurements, it has clear physical meaning connecting to the Landauer approach [34], and thus provides a physically meaningful trend. As will be manifest in Part II [29], in the sub-10-nm technology nodes where the space becomes very limited, the device parasitic, tunneling leakage, and the SCE become so significant that the device has to be carefully designed. Therefore, the emphasis of this paper is on the scaling trend rather than the accuracy in absolute values.

A. Inversion Gate Capacitance (C_{inv})

In a MOSFET, the mobile charge density in strong inversion at the VS, where the gradual channel approximation applies [34], can be approximated as $Q_{\rm xo} \approx -C_{\rm inv} \cdot (V_{\rm gs} - V_t)$, where $C_{\rm inv} = C_{\rm ox} \cdot C_s(C_{\rm ox} + C_s)$, $C_{\rm ox}$ is the gate oxide capacitance, and C_s is the semiconductor capacitance [35]. In planar bulk semiconductor materials, the DOS is usually so large that $C_s \gg C_{\rm ox}$ and $C_{\rm inv} \approx C_{\rm ox}$; however, for CNTs, the CNT quantum capacitance (C_q) needs to be considered because C_q is comparable with $C_{\rm ox}$ due to the relatively low DOS. Strictly speaking, C_q is bias-dependent [36]. However, the numerical simulation in Fig. 2(a) shows that the linear relation between $Q_{\rm xo}$ and $V_{\rm gs} - V_t$ in the inversion

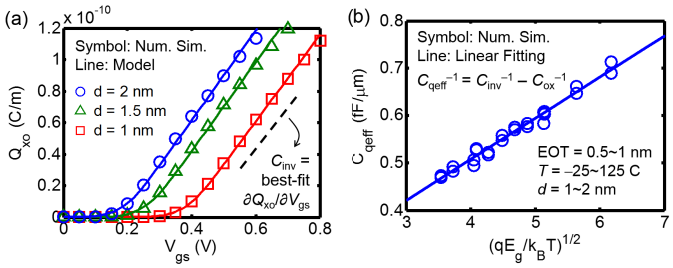

Fig. 2. (a) Comparison of the VS carrier density $Q_{\rm xo}$ versus $V_{\rm gs}$ between the numerical simulation [37] and the model (see Section II-A and [23]). EOT = 0.7 nm. (b) Effective CNT quantum capacitance $C_{\rm qeff}$ versus $\sqrt{(qE_g/k_BT)}$ extracted from the numerical simulation [37] for various temperatures, EOT's, and CNT diameters.

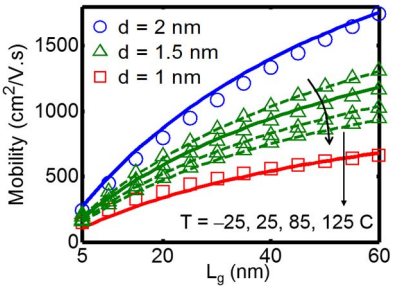

Fig. 3. Low-field mobility versus L_g for different CNT diameters and temperatures. The symbols are the peak mobility given by (3) and lines represent the model given by (2). The mobility decreases toward smaller L_g, as the conductance becomes constant with quasi-ballistic transport, see (3).

region is still retained over a reasonable range of $V_{\rm gs}$ and $Q_{\rm xo}$, implying the viability of having a constant effective C_q ($C_{\rm qeff}$) to account for the effect of quantum capacitance in the calculation of $C_{\rm inv}$. In the VS-CNTFET model, $C_{\rm inv}$ is calculated as follows:

$$C_{\rm inv} = C_{\rm ox}C_{\rm qeff}/(C_{\rm ox} + C_{\rm qeff}) \tag{1a}$$

$$C_{\rm qeff} = c_{\rm qa}\sqrt{q \cdot E_g/(k_BT)} + c_{\rm qb} \tag{1b}$$

$$C_{\rm ox} = 2\pi k_{\rm ox}\varepsilon_0/\{\ln[(2t_{\rm ox} + d)/d]\} \tag{1c}$$

where q is the elementary charge, T is the temperature in Kelvin, k_B is Boltzmann's constant, $c_{\rm qa}$ and $c_{\rm qb}$ are the empirical fitting parameters, $C_{\rm ox}$ is the gate oxide capacitance of a GAA structure, ε_0 is the permittivity in vacuum, and $t_{\rm ox}$ and $k_{\rm ox}$ are the thickness and the relative dielectric constant of the gate oxide, respectively. Equation (1b) is inspired by the theory that the maximum CNT C_q is approximately proportional to $(E_g/T)^{1/2}$ [36], and $c_{\rm qa} = 0.087$ fF/μm and $c_{\rm qb} = 0.16$ fF/μm are determined empirically in Fig. 2(b) by fitting (1b) to the $C_{\rm qeff}$ extracted from a numerical simulator provided by [37], which simulates a GAA-CNTFET with heavily doped S/D regions, and the carrier transport is simulated based on the NEGF formalism. In Fig. 2(a), the modeled $Q_{\rm xo}$ is calculated by substituting (1) into the equations in [23, eq. (1.3)] and compared with the numerical simulation for different CNT diameters.

B. Carrier Mobility (μ)

As L_g scales down to nanoscale, the carrier transport approaches the ballistic limit and carrier scattering in the channel becomes less significant. In this paper, the mobility is the so-called apparent mobility [34], a concept that connects the ballistic and diffusive regimes. The apparent mobility could also be understood as another way to express the mean free path (MFP). As device dimensions become smaller than the MFP, the carriers travel across the channel nearly without scattering and scatter only at the source and drain. In this context, the MFP becomes the channel length. In the VS-CNTFET model, μ is modeled empirically as follows:

$$\mu = \mu_0 L_{\rm g}(d/d_{00})^{c_\mu}/(\lambda_\mu + L_g) \tag{2a}$$

$$\mu_0 = \mu_{00} - t_\mu T \tag{2b}$$

$$\lambda_\mu = \lambda_{00} - t_\lambda T \tag{2c}$$

where d is normalized to $d_{00} = 1$ nm to become dimensionless, and t_μ, t_λ, μ_{00}, λ_{00}, and c_μ are empirical fitting parameters to capture the dependence on temperature, gate length, and CNT diameter. To validate (2) and determine the fitting parameters, the 1-D quantum transport theory at low fields is used, written here for the lowest subband [16], [38]

$$G = \frac{4q^2}{h}\int_{E_c}^{\infty} \frac{\lambda_i(E,T,d)}{L_g + \lambda_i(E,T,d)}\left[-\frac{\partial f(E,E_F)}{\partial E}\right]dE \tag{3}$$

where G is the CNT conductance, h is Planck's constant, E_c is the conduction band edge, E is the energy of free electrons, E_F is the Fermi level, f is the Fermi–Dirac distribution function, and λ_i is the MFP in CNTs representing the aggregate effect of optical and acoustic phonon scattering. The expression for λ_i, its experimental validation, and treatment across multiple subbands have been detailed in [38] (only the lowest subband is considered here). Due to the complex expression for λ_i, (3) cannot be integrated analytically; therefore, (2) is employed in the VS-CNTFET model instead to avoid the use of a numerical integral. Fig. 3 shows the comparison between the analytical model given by (2) and the data-calibrated numerical model given by (3) for different L_g, d, and T, where $t_\mu = 3.38$ cm^{2}V^{-1}s^{-1}K^{-1}, $t_\lambda = 0.05$ nm/K, $\mu_{00} = 2388$ cm^{2}V^{-1}s^{-1}, $\lambda_{00} = 77$ nm, and $c_\mu = 1.37$ are extracted. The long-channel peak mobility decreases linearly with increasing temperature, consistent with the experimental observation in [39].

It should be noted that for device configurations similar to Fig. 1, the source and drain are in fact separated by $L_g + 2L_{\rm ext}$ rather than L_g. However, since the extensions are not gated and have higher doping densities than the region under the gate (thus different MFPs), we treat the extensions in [29] as extrinsic elements and confine the scope of intrinsic elements (described by the VS model) to the region under the gate, leading to a hierarchical model. In the experimental measurements, however, it is not easy to separate the region under the gate from the extensions and the contacts; hence, any extraction of mobility for a short-channel CNTFET from the I–V measurements is actually a reflection of the commingled behaviors of contact injection and carrier transport in the extensions and the channel. Therefore, the use of apparent mobility [34] in the VS model can be viewed as a convenience for describing the experimental I–V curves in a hierarchical model. We note that the apparent mobility approaches zero as

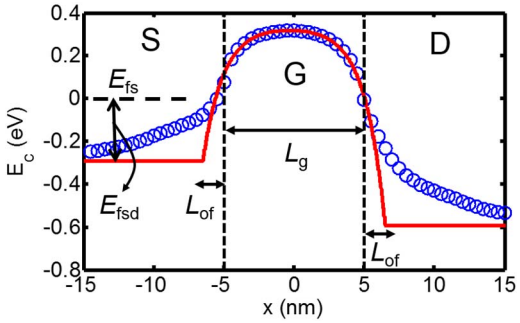

Fig. 4. Comparison of the conduction band profile between the numerical simulation [37] (symbols) and the model (line) given by (4) and (6).

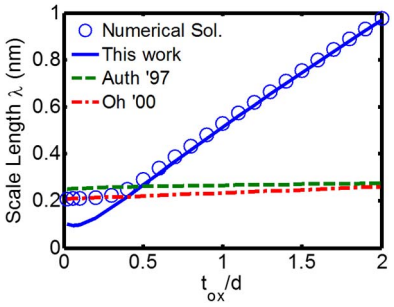

Fig. 5. Comparison of the scale length λ between the solution to (5) and the model given by (6) for $d = 1$ nm and $k_{ox} = 16$. Good agreement is observed for $t_{ox} > d/2$, while the approximation given in [42] works better for $t_{ox} < d/2$.

the channel length (which limits the MFP) approaches zero, consistent with the ballistic limit.

C. SCE Parameters (SS, DIBL, V_t Roll-Off)

The SCE is essentially the phenomenon of decreasing V_t and increasing the SS and DIBL as L_g scales down. In this paper, the SCE parameters are derived from a GAA cylindrical structure based on the scale length theory [40]. The first step is to model the E_c profile along the channel. In the subthreshold region, where the mobile charge in the channel is negligible, the E_c profile can be obtained by solving the Laplace equation, and the resulting E_c can be expressed as

$$E_c(x) = a_1 e^{-x/\lambda} + a_2 e^{x/\lambda} - V_{gs} + E_g/2 \tag{4}$$

where x is the direction along the channel, λ is the electrostatic scale length (also known as the screening length), and a_1 and a_2 are coefficients determined by the boundary conditions: 1) $E_c(-L_{of} - L_g/2) = -E_{fsd}$ and 2) $E_c(L_{of} + L_g/2) = -E_{fsd} - V_{ds}$, where L_{of} is an empirical parameter functioning like an extension of the L_g that captures the finite Debye length at the gate-to-S/D junctions, and E_{fsd} is the energy difference from the Fermi level to the E_c at the S/D extensions (see Fig. 4). All energies are referenced to the Fermi level at the source (i.e., $E_{fs} = 0$).

In a GAA cylindrical structure, λ is a solution to the Laplace equation in cylindrical coordinates satisfying the boundary condition at the CNT/oxide interface

$$\frac{Y_1(\zeta)}{J_1(\zeta)} = \gamma \frac{Y_0(\zeta)}{J_0(\zeta)} + (1-\gamma)\frac{Y_0(\zeta + t_{ox}/\lambda)}{J_0(\zeta + t_{ox}/\lambda)} \tag{5}$$

where J_m and Y_m are Bessel functions of the first kind and second kind of order m, $\gamma \equiv k_{cnt}/k_{ox}$, k_{cnt} is the relative dielectric constant of the CNT, and $\zeta \equiv d/(2\lambda)$. Equation (5) is a transcendental equation, which has no closed form solution for λ. Analytical approximations of λ in GAA-MOSFETs have been derived in [41] by assuming that the E_c profile is parabolic in the transverse direction; however for CNTFETs, d is often smaller than t_{ox}, so the approximation made in [41] fails. When $t_{ox} > d/2$, we show that λ can be approximated as

$$\begin{aligned} \lambda &= \frac{d + 2t_{ox}}{2z_0}[1 + b(\gamma - 1)] \\ b &= 0.41\left(\zeta_0/2 - \zeta_0^3/16\right)(\pi\zeta_0/2) \\ \zeta_0 &= z_0 d/(d + 2t_{ox}) \end{aligned} \tag{6}$$

where $z_0 \approx 2.405$ is the first zero of J_0. Derivation of (6) is detailed in [23, eqs. (15)–(19)]. Equation (6) is compared with the numerical solution to (5) in Fig. 5, showing good agreement when $t_{ox} > d/2$. When $t_{ox} \gg d$, (6) can be simplified to $\lambda \approx (d + 2t_{ox})/z_0$; on the other hand, when $t_{ox} \ll d$, it has been shown in [42] that $\lambda \approx (d + 2\gamma \cdot t_{ox})/z_0$. In both the extreme cases, λ increases linearly with d and t_{ox}. In this paper, $k_{cnt} = 1$ is used, assuming it is air inside the CNT [43]. However, different values of k_{cnt} from 5 to 10 for semiconducting CNTs have been reported both theoretically [44] and experimentally [45]. Nonetheless, we can show that (6) holds for a wide range of k_{cnt} (from $1 \sim 20$).

By substituting (6) into (4), the E_c profile is calculated and compared with the numerical simulation [37] in Fig. 4, showing good agreement in the gate region. Although the potential tails extending into the S/D extensions are not captured by (4), this will not affect the calculation of the SCE parameters, since only the top of the E_c (E_{cmax}) matters. Modeling of the tails will be discussed in [29] when calculating the tunneling currents. Once the E_c profile is known, the SCE parameters can be derived as

$$n_{ss} = -\partial E_{c\max}/\partial V_{gs}\big|_{V_{ds}=0} = (1 - e^{-\eta})^{-1} \tag{7a}$$

$$\delta = -\partial E_{c\max}/\partial V_{ds}\big|_{V_{ds}=0} = e^{-\eta} \tag{7b}$$

$$-\Delta V_t = E_g/2 - E_{c\max}\big|_{V_{ds}=0} = (2E_{fsd} + E_g)e^{-\eta} \tag{7c}$$

where $\eta \equiv (L_g + 2L_{of})/2\lambda$, and E_{cmax} is calculated by substituting $x = -\lambda/2 \cdot \ln(a_2/a_1)$ into (4). Equation (7) is compared with the numerical simulation in Fig. 6. Empirically, $L_{of} \approx t_{ox}/3$ is found to achieve the best fitting results. A physical interpretation of the relation between L_{of} and t_{ox} is that when t_{ox} becomes larger, the fringe field from the gate to the S/D extensions will extend, making L_{of} longer. Nevertheless, in general, L_{of} should be viewed as a fitting parameter. Note that (7) is a direct result of solving Poisson's equation without considering nonidealities such as oxide-CNT interface states. Therefore, SS $\approx$ 60 mV/decade and DIBL = 0 for long-channel devices. More discussion on the oxide-CNT interface is included in [29]. Although (7) is derived from a GAA structure, other device structures such as top gate and bottom gate should follow the same trend as long as a proper model for λ is used.

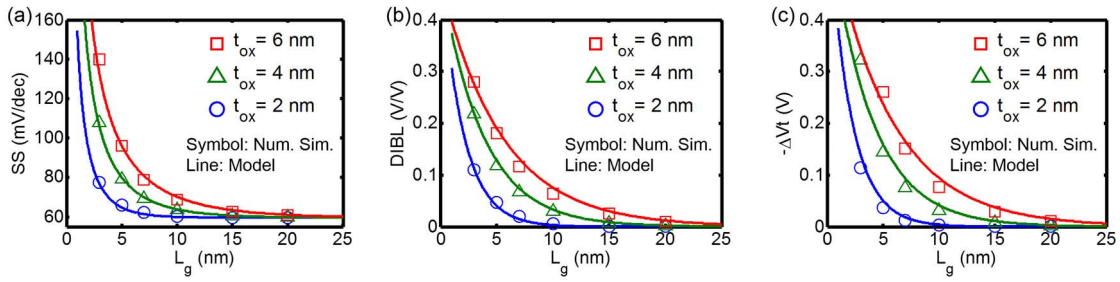

Fig. 6. Comparison of (a) SS, (b) DIBL, and (c) V_t roll-off between the numerical simulation [37] and the model given by (7) for different gate oxide thickness and $d = 1.3$ nm. Tunneling currents are excluded.

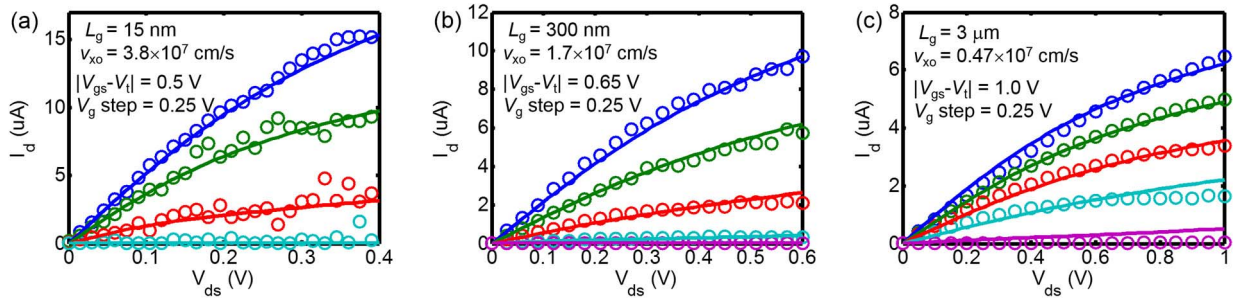

Fig. 7. Extraction of VS carrier velocity. The symbols are experimental data from [49]. (a) $v_{xo} = 3.8 \times 10^7$ cm/s for $L_g = 15$ nm. (b) $v_{xo} = 1.7 \times 10^7$ cm/s for $L_g = 300$ nm. (c) $v_{xo} = 0.47 \times 10^7$ cm/s for $L_g = 3$ μm. Note that the polarity of V_{gs} and V_{ds} are flipped compared to the original data to become n-type FETs.

D. Virtual Source Carrier Velocity (v_{xo})

The VS carrier velocity (v_{xo}), also known as the injection velocity, is one of the key metrics for the transistor technology [46]. v_{xo} can be associated with L_g through the theory of back scattering of carriers in the channel [47]

$$v_{xo} = \frac{\lambda_v}{\lambda_v + 2l} v_B \tag{8}$$

where v_B is the carrier velocity in the ballistic limit, λ_v is the carrier MFP, and l is the critical length defined as the distance over which the electric potential drops by $k_B T/q$ from the top of the energy barrier in the channel. Strictly speaking, l is proportional to L_g and dependent on V_{ds}, as described in [48]. However, since using a bias-independent v_{xo} can fit the experimental $I_d - V_{ds}$ data fairly well for different values of L_g (as will be seen shortly) and only a small range of L_g is of our interest (e.g., 5 nm $< L_g <$ 30 nm), here $l \approx L_g$ is assumed for the sake of simplicity and λ_v is thus empirical. To extract v_B and λ_v, the VS model [24] is fitted to the $I_d - V_{ds}$ data from [49], where three CNTFETs on the same substrate with identical structures but different gate lengths were measured.

The extraction flow of v_{xo} involves: 1) $d = 1.2$ nm, $L_g = 15$ nm/300 nm/3 μm, $R_s = 5.5$ kΩ, and SS = 135 mV/decade according to the reported experimental data in [49]; 2) estimating, due to lack of C–V data, $C_{ox} = 0.156$ fF/μm by simulating a metallic cylinder placed on a 10-nm-thick HfO_2 with a back gate using TCAD Sentaurus [50]; 3) $\mu = 255/10^3/2.1\times10^3$ cm^{2}V^{-1}s^{-1} for $L_g = 15$ nm/300 nm/3 μm, respectively, estimated by (3); 4) $\alpha = 3.5$ and $\beta = 1.8$ as suggested in [21]; and 5) the DIBL and V_t are treated as free parameters because the two parameters are susceptible to the oxide-CNT and air-CNT interface properties and may suffer from different degrees of the hysteresis effect [13]. In fact, the extracted v_{xo} is not sensitive to the choice for DIBL and V_t. Finally, v_{xo} is treated as a free parameter to achieve the best fitting result as shown in Fig. 7, with the VS parameters summarized in Table I. If uncertainty exists in the exact value of d due to the measurement, the values of C_{ox} and μ would be adjusted accordingly and the extracted v_{xo} could be slightly different, but the change will be minor and the scaling trend will remain the same. By fitting (8) to the extracted values of v_{xo}, $\lambda_v = 440$ nm and $v_B = 4.1 \times 10^7$ cm/s are extracted. v_{xo} for other materials has been extracted from devices at various values of L_g, including 1.35×10^7 cm/s for 32-nm L_g Si MOSFET [21] and 3.2×10^7 cm/s for 30-nm L_g III–V HFET [51].

TABLE I
VS PARAMETERS FOR DATA FITTING

Parameter	$L_g = 15$ nm	$L_g = 300$ nm	$L_g = 3$ μm
C_{inv} (fF/μm)	0.156		
v_{xo} (cm/s)	3.8	1.7	0.47
μ (cm^{2}V^{-1}s^{-1})	255	1000	2100
V_t (V)	1.27	1.21	1
SS (mV/dec)	135		
DIBL (V/V)	0.18	0.15	0.15
R_s (kΩ)	5.5		

To model the dependence of v_{xo} on CNT diameter, we refer to the carrier transport theory in MOSFETs [52]: the maximum value of v_{xo} is approximately the equilibrium unidirectional thermal velocity v_{Ti}. For the nondegenerate

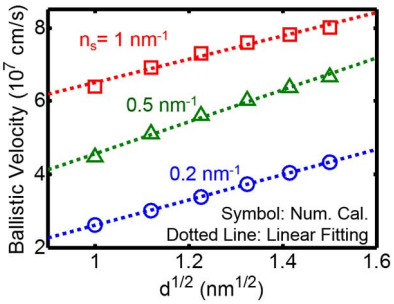

Fig. 8. Theoretical carrier velocity in the ballistic limit (symbols) versus the square-root of CNT diameter (dotted lines) for different carrier densities (n_s). The symbols are calculated by (9).

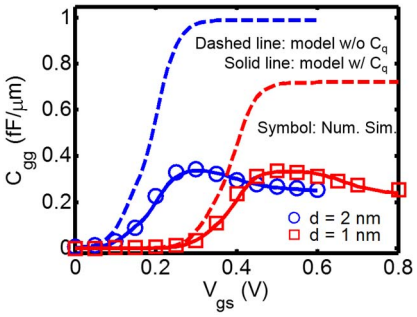

Fig. 9. Comparison of small-signal gate capacitances C_{gg} between the numerical simulation [37] and the model given by (10) at $V_{ds} = 0$. The dashed lines represent the case where CNT quantum capacitance is not considered.

case, $v_{Ti} = 2k_BT/(\pi m^*)$, where $m^* = h^2/(9\pi^2 a_{cc} E_p d)$ is the effective mass in CNTs [36]. Therefore, we can express $v_B = v_{B0}(d/d_0)^{1/2}$, where $v_{B0} = 4.1 \times 10^7$ cm/s and $d_0 = 1.2$ nm are extracted from [49] set as reference points. To examine the validity of the linear relation between v_B and $d^{1/2}$, the 1-D Landauer formula [16] is used to calculate the theoretical ballistic velocity v_{Bth}

$$I_{dB} = \frac{4q}{h}\int [f_S(E) - f_D(E)]\,dE = \frac{4q}{h}k_BT \ln\left[\frac{1+\exp\left(\frac{\psi_s - E_g/2q}{k_BT/q}\right)}{1+\exp\left(\frac{\psi_s - E_g/2q - V_{ds}}{k_BT/q}\right)}\right] \quad (9)$$

where I_{dB} is the drain current in the ballistic limit calculated by the 1-D Landauer formula, and $v_{Bth} = I_{dB}/n_s$, where n_s is calculated by (2b). Fig. 8 shows v_{Bth} versus $d^{1/2}$ for different carrier densities, indicating that the linear relation between v_{Bth} and $d^{1/2}$ holds for a wide range of d and n_s.

III. Terminal Charge Model

Proper modeling of the terminal charges is required to account for the dynamic operation of an FET. Under quasi-static conditions, the partitioning of charges at the source (q_s) and the drain (q_d) is accomplished through the Ward-Dutton charge-partitioning scheme [53], and the derivative of terminal charges with respect to the terminal voltage gives the small-signal capacitances [54]. In a short-channel MOSFET, the carrier transport generally falls somewhere in between the drift-diffusion regime and the ballistic transport regime. The charge model employed in this paper is similar to the VS charge model introduced in [55], in which carrier transport is assumed to be diffusive when V_{ds} approaches zero and ballistic when V_{ds} approaches infinity. The charges in the two extreme cases are computed separately and then combined through a V_{ds}-dependent smoothing function. Due to the limited space, the complete derivation of the charge model is detailed in [23, pp. 21–24]. This section focuses on a correction term in the charge model to account for the effect of CNT C_q.

As described in [36, Ch. 6.7], the CNT C_q increases as V_{gs} increases from zero to V_t, reaches a maximum, and finally decreases asymptotically to $C_{qinf} \equiv 8q^2/(3a_{cc}\pi E_p)$ as $V_{gs} \to \infty$, when only the first subband is considered. The decrease in C_q is because of the rapid drop of CNT DOS after the van Hove singularity [31]. The effect of C_q is not considered in the VS charge model originally developed for silicon MOSFETs. While an analytical model for C_q of CNTs has been developed in [19], the equations are relatively complex, making analytical expressions for q_s and q_d hard to obtain. Here, the terminal charge is modeled phenomenologically rather than from the first principles to account for the effect of C_q

$$q_{ch} = -L_g\,(Q_{xo} - Q_{xob}) \quad (10a)$$

$$Q_{xob} = (C_{inv} - C_{invb}) \cdot n_{ss}\phi_t \cdot \ln\left(1 + \exp\frac{V_{gs} - \left[V_{tb} - \alpha \cdot \phi_t \cdot F_f\,(V_{tb})\right]}{n_{ss} \cdot \phi_t}\right) \quad (10b)$$

$$C_{invb} = C_{ox} \cdot C_{qinf}/(C_{ox} + C_{qinf}) \quad (10c)$$

where q_{ch} is the total channel charge proportional to q_s and q_d (see [26, eqs. (44) and (50)]), $\phi_t = k_BT/q$ is the thermal voltage, Q_{xob} serves to gradually decrease the absolute value of q_{ch} around V_{tb}, and V_{tb} is a fitting parameter to be determined. Here, we discuss a special case of $V_{ds} = 0$ to demonstrate how the model works. At $V_{ds} = 0$, $q_s = q_d = q_{ch}/2$, and the small-signal gate capacitance $C_{gg} = -1/L_g \cdot (\partial q_{ch}/\partial V_{gs})$. When $V_{gs} < V_t$, $Q_{xo} \approx 0$, $Q_{xob} \approx 0$, and $q_{ch} \approx 0$; as V_{gs} increases to $V_t < V_{gs} < V_{tb}$, $|Q_{xob}| \ll |Q_{xo}|$, so $q_{ch} \approx -L_g Q_{xo} \approx -L_g C_{inv}(V_{gs} - V_t)$, and C_{gg} approaches the peak value C_{inv}; when $V_{gs} \gg V_{tb}$, Q_{xob} becomes appreciable and $q_{ch} \approx -L_g\{C_{inv} \cdot (V_{tb} - V_t) + C_{invb} \cdot (V_{gs} - V_{tb})\}$, and $C_{gg} \approx C_{invb}$, as expected when V_{gs} approaches infinity. The modeled C_{gg} is compared with the numerical simulation [37] in Fig. 9, where $V_{tb} = 0.7E_g/q + 0.13$ is determined empirically to achieve the best fitting result. Compared with the case, where quantum capacitance is not considered, the C_{gg} including the quantum capacitance is lower and gradually decreases at high V_{gs}. The resulting charge model is consistent with the current model because they share the same V_t and Q_{xo}.

IV. CNTFET Intrinsic Performance and CNT Diameter

In this section, the impact of CNT diameter on the intrinsic CNTFET performance is evaluated based on the model

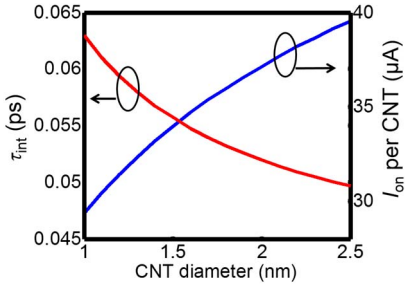

Fig. 10. Intrinsic on-state current I_{on} and gate delay τ_{int} versus CNT diameter at $L_g = 8$ nm and $V_{dd} = 0.71$ V. A 2-nm diameter CNT has 27% higher I_{on} and 21% lower τ_{int} than a 1-nm diameter CNT due to higher mobility, carrier velocity, and gate capacitance.

described in Sections II and III. Inputs to the VS-CNTFET model are: 1) $L_g = 8$ nm; 2) supply voltage $V_{dd} = 0.71$ V; and 3) equivalent oxide thickness (EOT) = 0.51 nm, selected from the 2023 node of the 2013 International Technology Roadmap for Semiconductors projections [56] which predicts the metal-1 pitch will be scaled down to 25.2 nm in 2023 for high performance logic; a GAA structure is assumed; and $R_s = R_Q/2 = h/(2q^2) \approx 3.3$ kΩ per CNT is added to the source and the drain terminals (see Fig. 1) to account for the quantum resistance associated with the interfaces between the 1-D CNT channel with the metal S/D contacts (including the lowest band double degeneracy with two spins) [36].

In Fig. 10, the ON-state current $I_{on} \equiv I_d(V_{gs} = V_{ds} = V_{dd})$ per CNT and the intrinsic delay $\tau_{int} \equiv L_g C_{inv} V_{dd}/I_{on}$ are plotted against the CNT diameter at a fixed OFF-state current $I_{off} \equiv I_d(V_{gs} = 0, V_{ds} = V_{dd}) = 1$ nA per CNT. As shown in Fig. 10, a 2-nm-diameter CNT can deliver 27% higher I_{on} and 21% lower τ_{int} than a 1-nm-diameter CNT. While $\mu \sim d^2$ has been observed experimentally in CNTFETs with relatively long channels ($L_g > 4$ μm) [39], here, we predict the ratio of $I_{on}(d = 2$ nm) over $I_{on}(d = 1$ nm) to be 1.27, much smaller than $2^2/1 = 4$, because the channel has become nearly ballistic at $L_g = 8$ nm. The increase in I_{on} for large-diameter CNTs is attributed to higher carrier mobility, velocity, and gate capacitance. The advantage of large-diameter CNTs in τ_{int} is not as prominent as in I_{on}, since the gate capacitance is also higher. As will be seen in [29], the CNT diameter has greater impacts on the parasitic contact resistance and the tunneling leakage currents in a highly scaled CNTFET.

V. Discussion

The VS carrier velocity is a crucial metric for the transistor technology because it directly determines the magnitude of the drive current as well as the delay of logic devices. A major advantage of the VS model is its capability of extracting v_{xo} directly from the measured data. Normally, the inversion gate capacitance C_{inv} is obtained from the C–V data. Then, with C_{inv} as one of the inputs, fitting the VS model to I–V data determines v_{xo} [57]. In other words, both I–V and C–V data are needed in order to reliably extract v_{xo}. For emerging devices like CNTFETs, however, reliable and reproducible C–V data are often hard to acquire, because of less understanding of the CNT-oxide and CNT-metal interfaces and the very small capacitance (aF range) of the 1-D channels [58], [59]. In this paper, numerical simulation by Sentaurus [50] is used to estimate the C_{inv} as a compromise for the extraction of v_{xo} in Fig. 7. In [24], $v_{xo} = 3 \times 10^7$ cm/s was extracted from a CNTFET with $L_g = 9$ nm [3], smaller than the $v_{xo} = 3.8 \times 10^7$ cm/s extracted from the $L_g = 15$ nm CNTFET in Fig. 7(a). While the contradiction (i.e., v_{xo} of a 9-nm-CNTFET is smaller than that of a 15-nm-CNTFET) might be attributed to the differences in gate oxide, fabrication conditions, CNT quality, or the long-range Coulomb interactions described in [60], the unexpected trend highlights the necessity for a larger number of consistent and systematic characterization of devices to extract v_{xo} in CNTFETs (e.g., CNTFETs built on the same CNT with different gate lengths below 100 nm). These high-quality device data are often not readily available because of the difficulties in device fabrication and the hysteresis and instability of experimental devices.

VI. Conclusion

The intrinsic elements of a compact CNTFET model based on the VS approach have been developed in this paper. A VS carrier velocity of 3.8×10^7 cm/s is extracted from recent experimental CNTFET with 15-nm gate length, providing evidence of the superior potential of CNTFETs for future transistor technology. The model captures dimensional scaling effects and is used to study the impact of CNT diameter on the intrinsic CNTFET performance, showing that a 2-nm-diameter CNT can deliver 27% higher intrinsic drive current than a 1-nm-diameter CNT at $L_g = 8$ nm. The VS-CNTFET model has been implemented in Verilog-A and is available online [23]. The model runs smoothly in the SPICE environment (as illustrated in [61]) because all the equations are analytical with no numerical iterations, and the output current is differentiable throughout all regions of operation. A more comprehensive analysis including nonideal contacts and tunneling leakage is carried out in [29].

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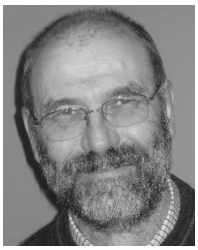

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