Achieving low-voltage thin-film transistors using carbon nanotubes

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The potential to perform at low voltages is a unique feature of carbon nanotube thin-film transistors (CNT-TFTs) when compared to more common TFT material options, such as amorphous Si or organic films. In this work, CNT-TFTs are fabricated using high-purity CNTs (verified electrically to be ~99% semiconducting) on an embedded gate device structure, which allows for scaling of the dielectric (equivalent oxide thickness ~ 3 nm) and yields a high gate capacitance. The high gate capacitance, coupled with the high semiconducting purity, leads to devices with excellent low-voltage performance having an average subthreshold swing of ~200 mV/decade (low of ~90 mV/decade) and on/off current ratios of 10^5. Testing hundreds of the CNT-TFTs on a chip at various channel lengths and widths provided a first look at the distribution of key performance metrics across a substrate. Favorable trade-offs between on-current and on/off current ratio were observed along with high field-effect mobility and narrow distributions in both the threshold voltage and subthreshold swing. The methods and results demonstrated here show that the low-voltage performance of CNT-TFTs is accessible for macroelectronic applications. © *2014 AIP Publishing LLC*.
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Thin-film transistors (TFTs) are ubiquitous structures used in the electronics industry for various macroelectronic applications including displays and sensors. Single-walled carbon nanotube (CNT) films are an excellent candidate for use as the channel material due to their superb electrical properties, mechanical flexibility, and compatibility with virtually any substrate.[1–11] Advances in solution processing, especially solution-based isolation of semiconducting CNTs, enables the fabrication of CNT-TFTs that outperform the industry standard, amorphous Si-TFTs. Such CNT-TFTs are fabricated using simple solution-based deposition techniques that are performed at room temperature and are compatible with virtually any substrate.[12–18]

Typical applications for macroelectronic devices and circuits (i.e., mobile and/or flexible displays, remote sensors, and circuits) will benefit from, and likely require, low-voltage performance as power is generally limited in their configurations. Low-voltage operation requires that the TFT switches to the on-state over a small gate voltage range and, additionally, has good transport properties to provide sufficient drive current. The subthreshold swing (*SS*) of a device characterizes how much gate voltage is needed to switch from the off- to the on-state, and the channel mobility is a good figure of merit for how much current the transistor can drive. Both *SS* and mobility are improved by the use of CNT-TFTs compared to other available solutions. While single-CNT devices—where the CNT channel(s) spans the source and drain—can exhibit excellent low-voltage performance,[19–22] CNT-TFTs typically have much larger subthreshold swings (~5–1 V/decade).[6,8,10,23,24] Exceptions to this trend in the literature are devices fabricated with self-assembled monolayer (SAM) based dielectrics[5] or ionic gel dielectrics where *SS* is reported as low as 130 mV/decade[25]—the fundamental limit at room temperature is 60 mV/decade. Although these examples demonstrate the ability of low-voltage performance, a route using a more conventional and scalable device architecture has been elusive. Furthermore, it is important to demonstrate the reproducibility of such low-voltage CNT-TFTs by examining large distributions of devices across a substrate.

In this work, semiconducting CNTs are used as the channel material for TFTs with an embedded gate structure that enables exceptional performance at low operating voltage with average *SS* of 200 mV/decade (as low as 90 mV/decade). The CNTs are sorted using column chromatography with a semiconducting purity greater than 99% verified both optically (UV-vis-NIR absorption spectroscopy) and with electrical measurements, as reported in an earlier work.[17] Raman spectroscopy on the CNT films confirms that additional defects are not introduced as a result of the solution processing. The embedded gate structure circumvents the difficult task of growing high quality dielectrics on carbon nanotubes;[26] allowing for employment of thin (10 nm) high quality HfO_2 films as the dielectric as well as the ability to gate the devices individually. The thin dielectric (equivalent oxide thickness (EOT) of approximately 3 nm) yields a large gate capacitance, enabling the low *SS*. The use of high-purity semiconducting carbon nanotubes coupled with the embedded gate structure results in the exceptional low voltage performance in these CNT-TFTs.

The device fabrication and layout are illustrated in Figure 1. The wafer consists of highly resistive silicon with 1 μm of thermally grown SiO_2. Gate trenches are patterned with photolithography followed by reactive ion etching (RIE) to produce 50 nm deep trenches in the SiO_2 (Figure 1(a)). The gate trench is then filled with tungsten metal and chemically mechanically polished (CMP) to planarize the

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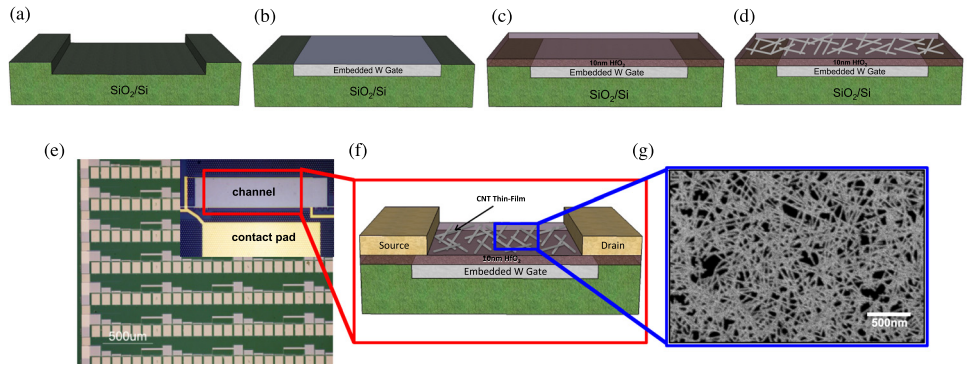

FIG. 1. Schematic of the process flow for embedded gate CNT-TFTs, including (a) the etching of the gate trench into the substrate, (b) filling and polishing of the W metal gate, (c) deposition via ALD of 10 nm of HfO_2, and the (d) modification of the gate oxide with poly-l-lysine followed by CNT deposition. The final device structure that includes the electrode deposition is illustrated in Figure 2(b). (e) An optical microscope image of an array of carbon nanotube thin-film transistors with varying lengths and widths and an (inset) image of a single CNT-TFT with a 10 μm channel length and an 80 μm channel width. (f) A schematic of a CNT-TFT illustrating the embedded gate structure, (g) a SEM image of a representative CNT film.

surface (Figure 1(b)). Atomic layer deposition (ALD) of 10 nm HfO_2 completes the gate stack (Figure 1(c)). The first three steps (Figures 1(a)–1(c)) were performed at wafer scale using a 200 mm CMOS line and then diced into individual chips prior to CNT deposition. Fabrication of this local-bottom gate (LBG) structure prior to CNT deposition obviates the need to grow a gate dielectric directly on the CNTs while allowing for individual gating of the devices. This is advantageous as growing high-quality, thin dielectrics on CNT films is extremely challenging due to a lack of reactive sites on the sp^2 bonded surface of the CNT. The HfO_2 surface is modified with poly-lysine (30% in water, Sigma-Aldrich), which aids in adsorption of the CNT network (Figure 1(d)).[6]

Large arrays of CNT-TFTs were fabricated with varying channel lengths and channel widths (as shown in Figure 1(e)) and designed to be compatible with a semi-automated probe station to allow for high-throughput characterization. After the CNT films are deposited, the channels are isolated via e-beam lithography to expose the areas of CNTs to be etched away outside of the channel. After etching of the unwanted CNTs in an oxygen plasma, the contacts (patterned *via* e-beam lithography) are metallized (Pd/Au). An estimated CNT density of ~8 CNTs/μm^2 is obtained after exposure to the semiconducting CNT solution for several hours as evidenced by the SEM image of Figure 1(g). The CNTs (ASP-100F, Hanwha Nanotech) are sorted (prior to device fabrication) by electronic type using column chromatography to isolate the semiconducting CNTs to purity levels >99%, as described in an earlier work.[17] Although the semiconducting fractions are screened using UV-vis-NIR absorption spectroscopy, the semiconducting purity is verified electrically by fabricating ~1000 individual CNT-FETs and counting how many are metallic or semiconducting.

Representative subthreshold and output curves of a CNT-TFT (channel length $L_{ch} = 5\ \mu m$, and width $W_{ch} = 80\ \mu m$) are shown in Figures 2(a) and 2(b), respectively. The subthreshold curves are well-behaved at varying drain biases (V_{ds}) from −1 V down to −100 mV, with minimal curve shifting and a steady *SS*. The on/off current ration (I_{ON}/I_{OFF}) is high (10^5) and consistent at various V_{ds}. Perhaps the most striking feature is that the *SS* is consistently low at varying drain bias with a value of ~200 mV/decade. This low *SS* coupled with the high I_{ON}/I_{OFF} and low threshold voltage (0.8 V) make these devices promising for low-voltage applications. The output curves (Figure 2(b)) show strong current saturation at $V_{DS} < 1$ V, with the linear behavior at low V_{ds} indicating Ohmic-like contacts.

As the channel lengths are several times larger than the average length of the CNTs (~500 nm), the devices operate in a percolation regime where the carriers transport across many CNTs to traverse the channel from source to drain. A

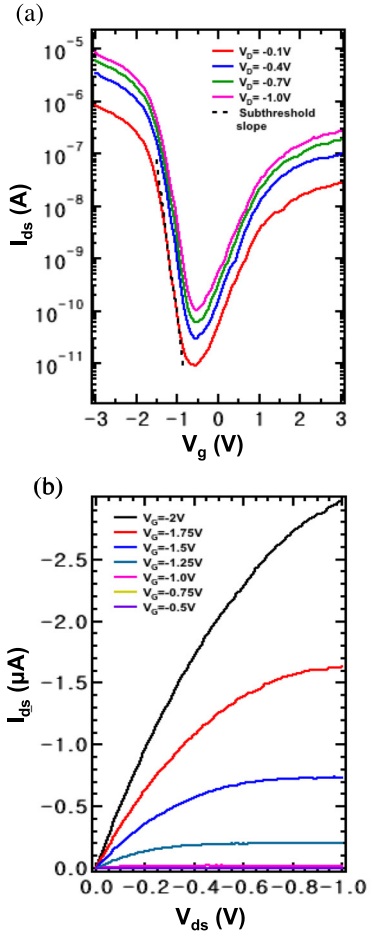

FIG. 2. (a) I_{ds} vs. V_g curve for a CNT-TFT with a channel length of 5 μm and a channel width of 80 μm at various drain-source biases. The dotted line indicates a subthreshold swing of 200 mV/dec. (b) I_{ds} vs. V_{ds} curve for the same CNT-TFT at various gate biases. The curves show clear saturation behavior and Ohmic-like contacts.

series of device performance parameters as a function of channel length are shown in Figures 3(a)–3(e). As expected, the on–current (Figure 3(a)) and peak transconductance (g_m in Figure 3(b)) both decrease with increasing channel length. This is due to the increasing number of CNT-CNT junctions present as L_{ch} is increased. Conversely, the I_{on}/I_{off} ratio increases dramatically with channel length from a value of 10 at L_{ch} of 1 μm to where it saturates at $\sim 10^5$. The slope of this increase is very sharp and indicative of the high level of purity of the semiconducting samples. The saturation of I_{ON}/I_{OFF} at $\sim 10^5$ is typical of CNTs in the larger diameter range, where the bandgaps are smaller, and is not due to the presence of metallic pathways.[24]

The field-effect mobility was calculated using gate capacitance values obtained through high-frequency electrical measurements. This allows for a precise calculation of the capacitance, and thus, the field-effect mobility.[7] Since the source/drain contacts overlap the gate dielectric, the measured capacitance was corrected to remove the parasitic capacitance between the gate metal and source/drain contacts. Because the source/drain contacts are narrow (300 nm) with respect to the device area, the correction is relatively small ($\sim$15%). The mobility is plotted versus channel length in Figure 3(d) and decreases slightly ($\sim$25%) as the channel length increases before saturating at $\sim 18\,cm^2V^{-1}s^{-1}$. The elevated mobility at small channel lengths is due to the presence of metallic pathways in the film at channel lengths of 1 μm. The subthreshold swing decreases slightly at L_{ch} from 1 μm to 5 μm before saturating at $\sim$200 mV/decade. This behavior is expected as the *SS* typically increases if the I_{ON}/I_{OFF} is small owing to a clipping of the off-state by the increased dominance of metallic CNTs. It is also worth noting that the spread in values for *SS* at channel lengths of 5 μm and above is small with a range of 90 mV/decade–320 mV/decade.

The device layout was designed such that several hundred devices could be measured using a semi-automated probe station to obtain statistics on device-to-device variability. Figures 4(a) and 4(b) are histograms of the number of devices versus threshold voltage (V_T) and *SS*, respectively.

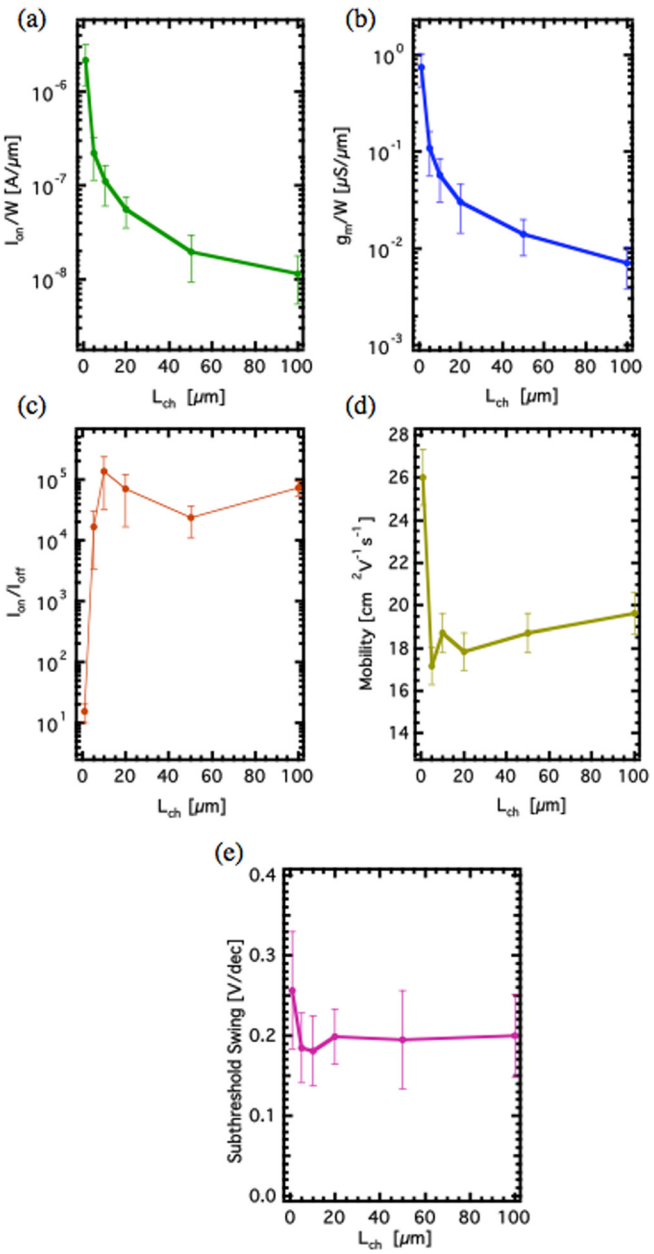

FIG. 3. Channel length dependence of the CNT-TFTs (channel width = 80 μm) on (a) I_{on}/W [A/μm], (b) g_m/W [μS/μm], (c) I_{on}/I_{off}, (d) mobility, and (e) subthreshold swing [mV/decade]. All the parameters presented here behave as expected from a device operating in the percolation regime.

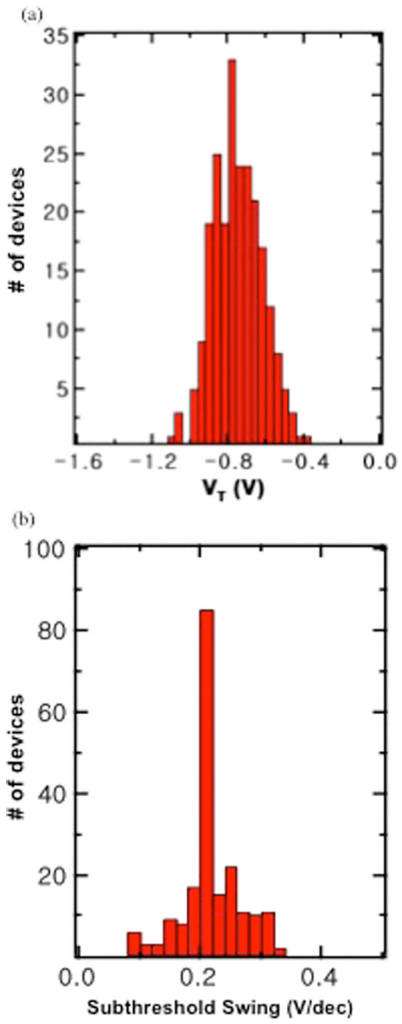

FIG. 4. (a) Histogram of V_T variation showing a relatively tight distribution and (b) histogram of the subthreshold swing yielding a tight distribution with a remarkably low value for devices of such large dimensions.

The V_T was centered at −0.8 V with relatively low variation (ranging from −0.4 V to −1.2 V). The *SS* displayed similar consistency and was centered at ~200 mV/dec.

Subthreshold swing can be expressed using the following equation:[11,27]

$$SS = \left(\frac{k_B T}{e}\right)\ln(10)\left(1 + \frac{C_{IT}}{C_i}\right),$$

where the value of *SS* above the room temperature limit of 60 mV/decade is determined by C_{IT}/C_i–C_{IT} is the capacitance resulting from interface traps, C_i is the gate capacitance, k_B is the Boltzmann constant, T is temperature, and *e* is the elementary charge of an electron. If C_{IT} is very small compared to C_i, then the *SS* approaches the limit of 60 mV/decade at room temperature. The C_{IT} is not greatly reduced in these devices versus previous literature results as similar dielectrics and interfacial organic layers are used. The dramatically reduced SS is more likely due to an increase in C_i as our dielectric thickness is greatly reduced and acts to screen out the effects of C_{IT}. The increased gate capacitance is enabled by the embedded gate geometry allow from extremely scaled dielectrics, and thus, high gate capacitance. This explanation is also consistent with the low *SS* values obtained from the devices with a monolayer dielectric and an ionic dielectric, both of which have high C_i.[5,25,28] These results demonstrate that one critical feature of low-voltage operation in CNT-TFTs is a high gate capacitance.

The exceptional low-voltage performance of these embedded gate CNT-TFTs is highlighted in the scatter plot (Figure 5) of *SS* versus I_{ON}/I_{OFF}. The goal is to push data points toward the bottom right of the plot, where the *SS* is low and the I_{ON}/I_{OFF} is high. The red points were taken from devices with varying channel lengths (5–100 μm) at a fixed channel width of 80 μm. Despite the varying I_{ON}/I_{OFF} (due to differences in channel length), the subthreshold swings are consistently small (~200 mV/dec) with high I_{ON}/I_{OFF}

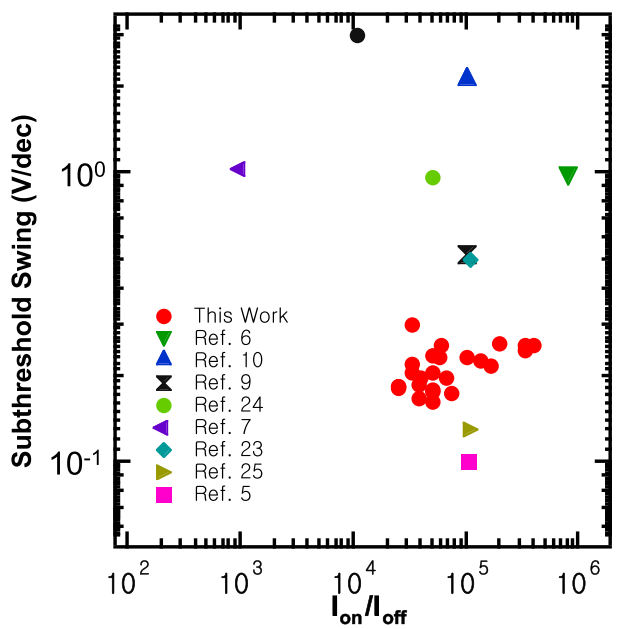

FIG. 5. (a) Plot of subthreshold swing versus I_{ON}/I_{OFF}. The data in red is from this work, while other data were extracted from I-V curves in literature references as noted.

obtained in longer (>5 μm) channel length devices. On the same plot, several representative CNT-TFT devices from key literature examples are also plotted. Although they have similar I_{ON}/I_{OFF} ratios, the subthreshold swings (extracted from the figures) are 2×–10× greater at the same I_{ON}/I_{OFF} ratios. This highlights the exceptional low voltage performance attained by coupling high-purity semiconducting CNTs with an embedded gate structure (which allows for thin EOT).

Exceptional low-voltage performance is demonstrated with CNT-TFTs that employ highly enriched semiconducting CNT solutions and embedded metal gate device geometry. Since the devices operate in the percolation regime, there are expected trade-offs between on-current and I_{ON}/I_{OFF} ratio. The device performance metrics (i.e., mobility, I_{ON}/I_{OFF}, g_M and *SS*) are competitive with, and in some cases better than, conventional thin-film technologies. The key to obtain low-voltage performance is dramatically increasing the gate capacitance to screen the capacitance generated by interfacial charge traps in thin film channel devices. These structures are ideally suited for macroelectronics that would benefit from operating at lower voltages to save on active power.

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