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Gate-Free Electrical Breakdown of Metallic Pathways in Single-Walled Carbon Nanotube Crossbar Networks

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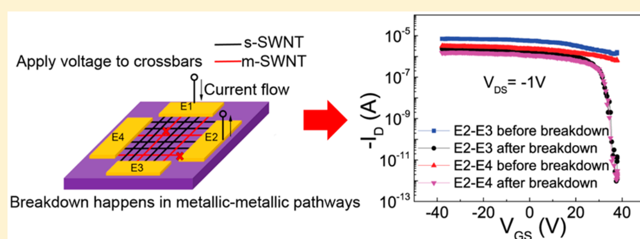
Supporting Information

ABSTRACT: Aligned single-walled carbon nanotubes (SWNTs) synthesized by the chemical vapor deposition (CVD) method have exceptional potential for next-generation nanoelectronics. However, the coexistence of semiconducting (s-) and metallic (m-) SWNTs remains a considerable challenge since the latter causes significant degradation in device performance. Here we demonstrate a facile and effective approach to selectively break all m-SWNTs by stacking two layers of horizontally aligned SWNTs to form crossbars and applying a voltage to the crossed SWNT arrays. The introduction of SWNT junctions amplifies the disparity in resistance between s- and m-pathways, leading to a complete deactivation of m-SWNTs while minimizing the degradation of the semiconducting counterparts. Unlike previous approaches that required an electrostatic gate to achieve selectivity in electrical breakdown, this junction process is gate-free and opens the way for straightforward integration of thin-film s-SWNT devices. Comparison to electrical breakdown in junction-less SWNT devices without gating shows that this junction-based breakdown method yields more than twice the average on-state current retention in the resultant s-SWNT arrays. Systematic studies show that the on/off ratio can reach as high as 1.4×10^6 with a correspondingly high retention of on-state current compared to the initial current value before breakdown. Overall, this method provides important insight into transport at SWNT junctions and a simple route for obtaining pure s-SWNT thin film devices for broad applications.



KEYWORDS: *Single-walled carbon nanotube, internanotube junction, gate-free, electrical breakdown, on/off ratio, thin-film transistors*

Single-walled carbon nanotubes (SWNTs) are known to be one of the most promising candidates for future nanoelectronics owing to their outstanding electrical properties.[1−7] Based on their electronic structure, SWNTs can be classified into semiconducting (s-) and metallic (m-) types. For application in logic gates, radio frequency devices and sensors, s-SWNTs are especially attractive owing to the presence of a sizable energy band gap. However, the coexistence of s- and m-SWNTs in prepared samples limits the application of SWNTs because the current through m-SWNTs can only be modulated very weakly, resulting in a high leakage current in field-effect transistors (FETs). Therefore, over the past decade, abundant research efforts have been made toward obtaining pure s-SWNTs.

One of the most commonly used strategies is to isolate s-SWNTs in solution phase and then deposit them onto target substrates.[3,8−11] However, the separation steps, which usually involve surfactant wrapping and sonication, can result in contamination, shortened nanotube length, higher defect density, and substantial bundling, thus reducing the quality of the SWNTs for device applications. Further, the controlled placement of s-SWNTs from solution phase is a formidable challenge that as yet requires significant improvement.[10,12,13]

As an alternative to solution-phase separation, SWNTs can be directly synthesized on surfaces by the chemical vapor deposition (CVD) method. This method not only provides the capability of maintaining the structural integrity of SWNTs but also allows for SWNT alignment in parallel arrays by using single crystalline substrates, such as quartz or sapphire.[14,15] However, s-SWNTs must be selectively synthesized or m-SWNTs selectively removed from the substrate. If all SWNTs are assumed to have equal opportunities to be nucleated, m-SWNT should account for 33% of CVD-SWNTs prepared. In recent years, based on the different reactivity between s- and m-SWNTs, great advancements have been made in selective s-SWNT growth via either in situ or postsynthesis purification, including using UV light,[16] H_2,[17] water,[18−20] methanol,[21] isopropanol,[22] oxidative catalyst support,[23] and NiO,[24] to exclusively etch away m-SWNTs from the mixed arrays. Despite this great progress, the reliable synthesis of 100% pure s-SWNTs remains evasive. In addition, how to prevent the formation of defects on s-SWNTs in a well-controlled fashion so as to avoid significant current drop in devices is also an open question.

The other effective strategy for purification of SWNTs bound to a substrate is to electrically break down the m-SWNTs in

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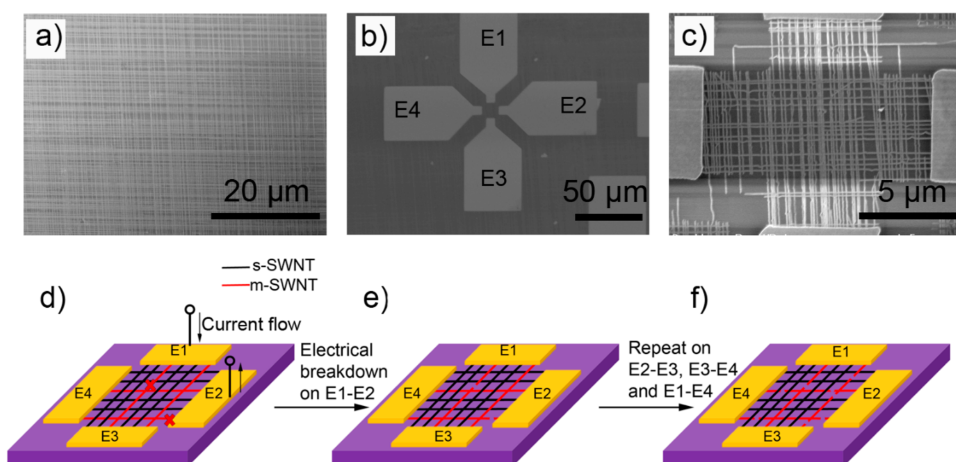

Figure 1. (a) SEM image of cross-stacked SWNT arrays. (b, c) Representative SEM images of a set of FETs based on as-prepared SWNT crossbars. Each aligned array is connected by a pair of electrodes with a channel length of 10 μm. The surrounding SWNTs outside of the channel area are removed by O_2 plasma etching. (d–f) Schematic illustration of the gate-free breakdown process on cross-stacked SWNT arrays: (d) a bias voltage is added between electrode E1 and E2 (device 0102) to trigger current-induced breakdown of metallic pathways. (e) After breakdown, open defects are created on m-SWNTs. (f) The breakdown process is repeated on device 0203, 0304, and 0104 to ensure sufficient breakdown of all metallic pathways.

devices using current-induced Joule heating. In 2001, Collins et al. first demonstrated the wall-by-wall electrical breakdown of multiwalled carbon nanotubes (MWNTs) by depleting semiconducting walls from charge carriers with a positive gate voltage.[25] This concept—taking advantage of differing heat generation in s- and m-SWNT—has been successfully extended to purifying SWNT arrays in later studies and has proven to be highly effective since it directly relies on the difference in electrical properties of s- and m-SWNTs.[6,26−28] Most of the reports involve the use of a transistor gate stack (dielectric and metal) and the application of an appropriate gate voltage to ensure the complete charge depletion in s-SWNTs; it was reported that, under nongating conditions (i.e., floating gate), s-SWNTs can still exhibit substantial conductance, compromising the selectivity of the breakdown process.[29] A disadvantage to the electrical breakdown method is the need for a bottom gate (the m-SWNTs must be exposed to reactant species in the air in order to break down, so a top gate will not suffice). Hence, the application of s-SWNTs on unconventional materials (e.g., plastic, flexible, and stretchable substrates) is restricted due to the absence of a back gate. Recently, Rogers group successfully demonstrated laser-[30] and microwave-[31] induced selective heating to m-SWNTs to expose them in a thermocapillary resist, followed by their removal using reactive ion etching. However, the density of SWNT arrays that can be purified by this method is limited by the width of trenches on the resist opened by the thermocapillary flow.[32] Therefore, it is highly desirable to develop a more accessible solution that allows exclusive breakdown of m-SWNTs in dense arrays and without gating.

For selective breakdown, it is necessary to properly control the current flow in s- and m-pathways so that they can be clearly distinguished. According to previous studies, the current in SWNT networks is limited by the Schottky barriers at s−m internanotube junctions,[33−35] and the resistance of such junctions is reported to be at least 1 order of magnitude higher than that of individual SWNTs.[36,37] Several groups have sought to utilize carrier transport at SWNT junctions by fabricating all-carbon nanotube FETs.[38−40] Other studies have shown the ability to improve device performance via nano-soldering at SWNT junctions.[41,42] In this work, a unique implementation of SWNT junctions provides a facile, effective, clean, and gate-free method to selectively break down m-SWNTs by flowing current through perpendicularly cross-stacked SWNT arrays. The present approach uses an amplification of the difference in Joule heat generation in m- and s-pathways by introducing junctions, which allow for complete breakdown of m-SWNTs while keeping s-SWNTs intact, without gating. By adding voltage to SWNT junctions, significant increases in on/off current ratios of not only junction-based but also junction-less devices can be achieved, and the on/off ratio after breakdown can reach as high as 1.4×10^6 with a current retention of ∼50%. Our systematic studies show that the junction-based electrical breakdown is much more selective than directly adding voltage across junction-less SWNT arrays without gating. Furthermore, the behaviors of three types of junctions (s−s, s−m, and m−m) are carefully investigated to reveal fundamental aspects of the gate-free breakdown mechanism. This study provides better understanding of SWNT junctions and a promising way to produce pure s-SWNTs for future device applications.

Results and Discussion. *Operation Principle of Junction-Based Electrical Breakdown.* For the fabrication of cross-stacked SWNTs, two layers of horizontally aligned SWNT arrays (∼4−6 SWNTs/μm), synthesized using a previously reported method,[21] are transferred from the quartz growth substrate to a silicon substrate having 280 nm SiO_2. The second SWNT array is oriented perpendicular to the first layer, forming a crossbar structure. Figure S1a in Supporting Information (SI) shows the diameter distribution of the SWNTs measured by atomic force microscope (AFM) with an average and standard deviation of 1.82 and 0.49 nm, respectively. Based on the diameter distribution, the band gap range of SWNTs used in our study is estimated to be 0.3−0.9 eV.[43] The frequently detected RBM peaks using Raman spectroscopy confirm that as-prepared nanotubes are all single-walled (Figure S1b). A representative scanning electron microscope (SEM) image of the cross-stacked SWNTs is shown in Figure 1a. Four electrodes (1.2 nm Ti/20 nm Pd/40 nm Au) are deposited to connect the two aligned arrays and photolithography

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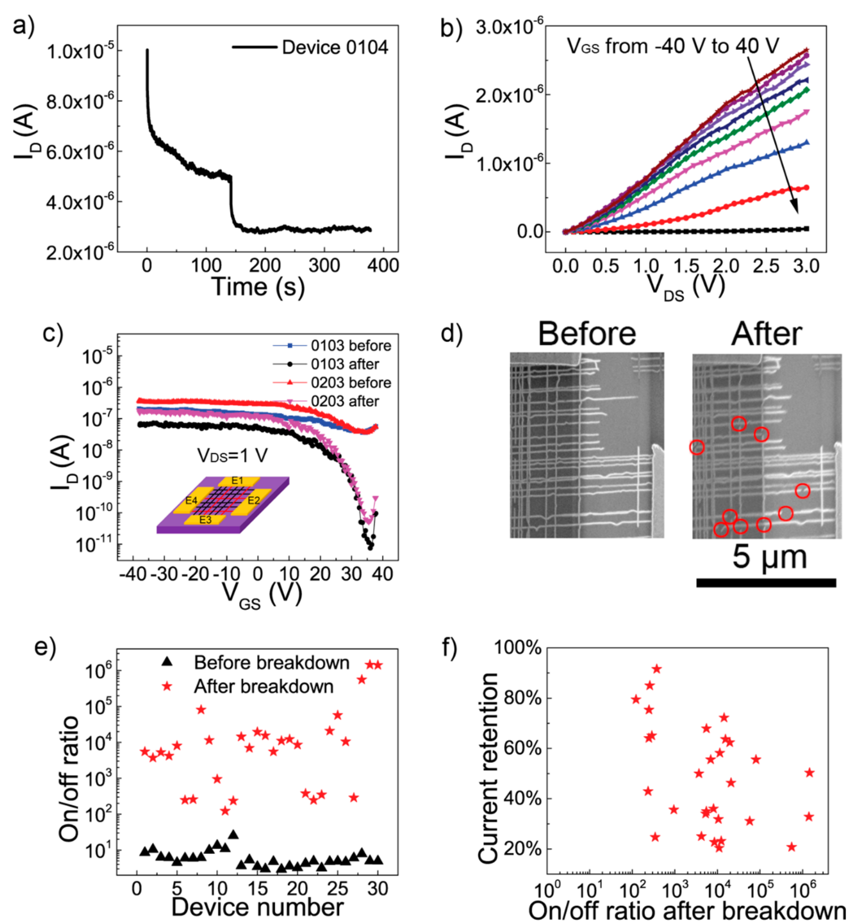

Figure 2. (a) Current versus measurement time of a crossbar junction-based FET under a fixed bias voltage (20 V) during the electrical breakdown process. The sudden drops in I_D indicate breakdown events. (b) Output characteristics of a representative device after electrical breakdown. V_{GS} varies from −40 to 40 V with a step of 10 V. (c) Subthreshold curves of a junction-less FET (device 0103) and a junction-based FET (device 0203) from the same group before and after electrical breakdown (V_{DS} = 1 V). (d) SEM images showing SWNTs in the representative device before and after electrical breakdown. Open defects of SWNTs are indicated by the red circles. (e) Display of on/off current ratios of devices (including 20 crossbar junction devices and 10 junction-less devices) before and after the junction-based electrical breakdown. (f) The on-state current retentions of devices in panel e as a function of the on/off ratios after electrical breakdown.

followed by O_2 plasma exposure is used to remove SWNTs outside of the channel (Figure 1b and c). A schematic illustration of the gate-free breakdown process for as-prepared devices appears in Figure 1d−f. First, as indicated in Figure 1d, a source−drain voltage is applied to electrodes E1 and E2 and maintained to allow the stepwise breakdown of SWNTs. It is clear that from E1 to E2, all charge carriers need to go through at least one SWNT junction and the metallic pathways formed by two metallic nanotubes (m−m junctions) carry much higher current than those involving s−m or s−s junctions. To ensure a complete breakdown of the metallic pathways, such a "burning" process is repeated between electrodes E2−E3, E3−E4, and E1−E4 (Figure 1f). More experimental details can be found in the method section in SI where the process flowchart of the breakdown process is shown in Figure S2. As a consequence, after the breakdown treatment, increases in the on/off current ratios of transistors are observed not only in the junction-based devices (named as devices 0102, 0203, 0304, and 0104) but also in the junction-less devices (0103 and 0204).

Efficiency and Selectivity. The electrical properties of two representative devices from the same group before and after breakdown, following the procedures mentioned above, are illustrated in Figure 2. Figure 2a shows the drain current (I_D) of a crossbar junction FET versus time under a fixed source−drain bias voltage (20 V). Abrupt drops in I_D) correspond to breakdown events. Similar current drop trends are also observed in the other 3 crossbar junction devices from the same group. Our empirical observation suggests that the decrease of I_D) to 1/6−1/3 of the starting current value is an appropriate range for the selective elimination of the metallic pathways (see method section in SI for details). The output characteristics of a representative device after breakdown is provided in Figure 2b. Figure 2c shows the subthreshold curves of device 0103 (junction-less) and 0203 (junction-based) before and after the electrical breakdown. Interestingly, the junction-less device (0103) exhibits a lower on-state current before and after breakdown compared to the crossbar device (0203), which might be attributed to (1) a slightly lower number of SWNTs in the 0103 array compared to 0204 and (2) shorter channel lengths for the s-SWNTs in the 0203 branch via conduction through m-SWNTs. To analyze the on/off current ratio, V_{GS} sweeping from 40 V to −40 V is used. In the two representative devices shown in Figure 2c, the on/off ratios increased from 4.5 and 10.4 to 8.1 × 10^3 and 3.7 × 10^3 with current retentions (defined as $I_{on\text{-}after}/I_{on\text{-}before}$) of 36% and 50%, respectively. These on/off ratios represent the complete breakdown of all metallic pathways because the minimum current in the off-state is smaller than that of a single metallic

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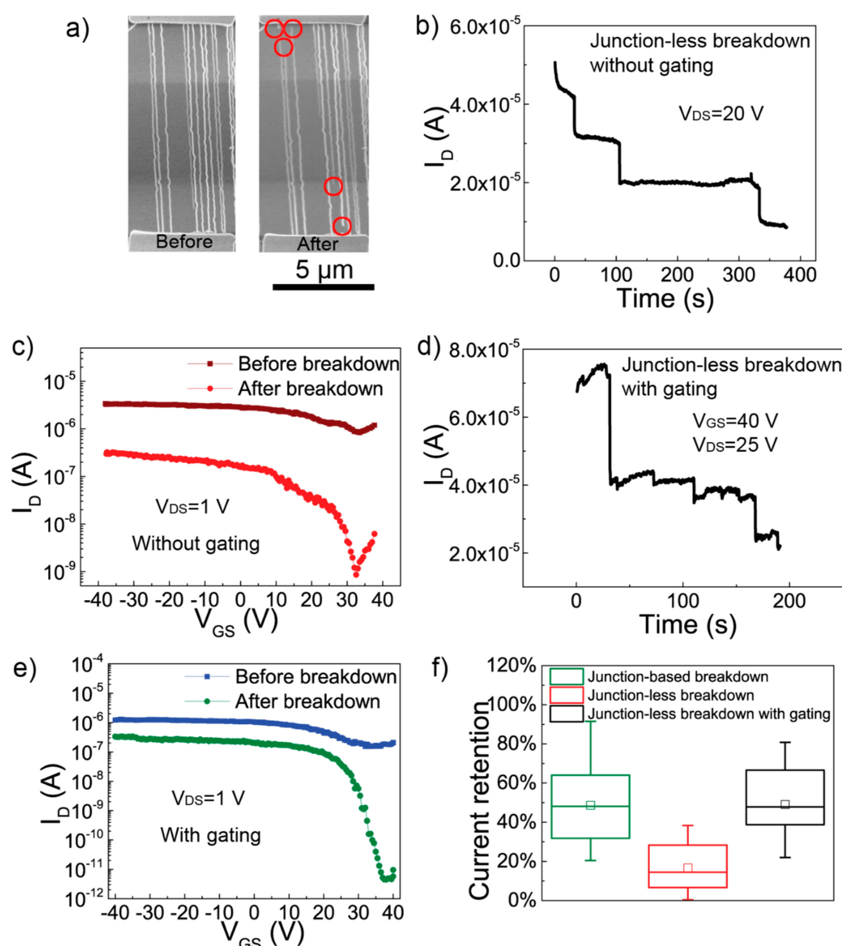

Figure 3. (a) SEM images of a representative device before and after the junction-less breakdown. The defects of SWNTs are marked by the red circles. (b) Source−drain current as a function of time during the junction-less breakdown without gating. The current drops to ∼1/5 of the initial value. (c) Subthreshold curves of the representative device before and after the junction-less breakdown without gating (V_{DS} = 1 V). The on-state current degrades to ∼10% of the initial value. (d) Source−drain current as a function of time during the junction-less breakdown with gating (V_{GS} = 40 V). (e) Subthreshold curves of a representative device before and after junction-less breakdown with gating. (f) Statistics of current retentions for junction-based breakdown (green) and junction-less breakdown without (red) and with (black) gating. The large boxes represent the percentage from 25% to 75%. The error bars represent the minimum and maximum values. The mean values are indicated by the small squares.

pathway. Figure 2d shows SEM images before and after breakdown with the open defects of SWNTs indicated by red circles.

To be more rigorous, devices with similar densities in the two crossing arrays were tested, and the on/off ratios of all devices, including junction-based and junction-less, before and after breakdown are plotted in Figure 2e. All of the devices demonstrate significant increase in the on/off ratio after the breakdown process, with the median shifting from 5.1 to 7.5 × 10^3. Considering the fact that each device contains no more than 30 SWNTs (average: 11), it is safe to conclude that metallic pathways are completely cut off. It should also be noted that several devices in Figure 2e demonstrate relative low on/off ratios(<200:1 junction-based; 200−500:4 junction-based and 3 junction-less), which is due to the higher percentage of semimetallic SWNTs (SWNTs with small but finite band gaps) contained in the corresponding FETs. Our results show that these devices can eventually be purified to reach higher on/off ratio levels by applying either a longer breakdown time or a higher breakdown voltage. Figure S3 illustrates examples of such a case, where the on/off ratios of a junction-based device and a junction-less device are increased from ∼200 after the first breakdown cycle (Figure S3a) to 3.1 × 10^4 and 1.9 × 10^3 after the second cycle (Figure S3b).

Figure 2f shows the on-state current retentions of all devices in Figure 2e as a function of the on/off ratios after electrical breakdown. The average and median values of the current retention are 49% and 44%, respectively, which are reasonable for the preservation of most s-SWNTs if we assume that about 2/3 nanotubes are s-SWNTs which carry somewhat smaller current than m-SWNTs because of the higher contact resistance.[44] The highest on/off ratio after breakdown is achieved when a negative bias voltage (−1 V) is used during the measurement as it supports the more favorable injection of holes into the valence band at the source with a smaller barrier height than electron injection into the conduction band. As shown in SI Figure S4, the on/off ratios of a junction-based and a junction-less FET both reach ∼1.4 × 10^6 with the current retention of ∼33% and ∼50%, respectively.

To further investigate the influence of SWNT density on the breakdown efficiency and selectivity, the same approach was also applied on SWNT crossbars with a density twice or three times (10−15 SWNTs/μm) higher than those used above (see Figure S5a in SI for SEM image), and it is found that this method is still effective. For these higher density crossbar

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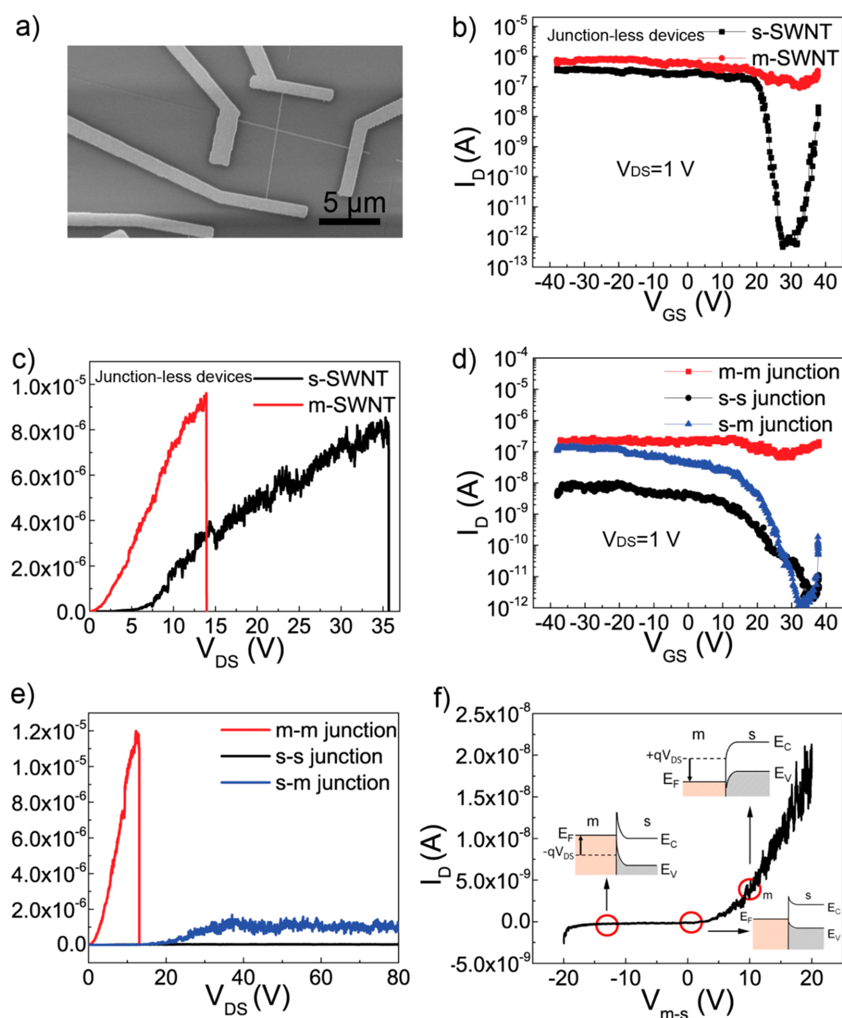

Figure 4. (a) SEM image of a representative device with a single junction formed by two individual SWNTs. (b) Subthreshold curves of junction-less devices: an s-SWNT (black) and an m-SWNT (red) (V_{DS} = 1 V). (c) Electrical breakdown curves of the junction-less devices in panel b. (d) Subthreshold curves of m−m (red), s−m (blue), and s−s (black) junctions formed by individual SWNTs (V_{DS} = 1 V). (e) Electrical breakdown curves of the three junctions shown in panel d. (f) $I-V$ curves of an s−m junction showing asymmetric transport behavior (insets: corresponding schematic band diagrams at the s−m junctions under zero, positive, and negative bias). Here the bias voltage (V_{m-s}) is applied to the m-SWNT while the s-SWNT is grounded. The Fermi level, conduction band, and valence band are marked as E_F, E_C, and E_V, respectively.

arrays, it is necessary to start with a lower breakdown voltage to avoid damages to s-SWNTs caused by correlated breakdown.[45] As shown in Figure S5b in SI, current drops start to be observed in a representative device when 10 V is applied for breakdown instead of 20 V as was used for the arrays with lower density. The application of 15 V allows the complete breakdown of all m-pathways (see Figure S5c in SI) to obtain high on/off ratios for both the junction-based (8.4×10^3) and junction-less (4.7×10^3) devices with a current retention of 53% and 60%, respectively (Figure S5d). However, performing junction-based breakdown on such dense crossbars with V_{DS} above 25 V increases the possibility of deactivating s-SWNTs. Considering that no gate is present in our breakdown method, we believe that it is crucial to limit the operating voltage to avoid damages to s-SWNTs for higher density SWNT arrays.

It should also be noted that, in order to achieve the best results, similar numbers of SWNTs in each of the crossbar arrays (i.e., devices 0103 and 0204) are preferred. This is because during the junction-based breakdown process, when the two arrays carry the same level of current and the resistances differ greatly, the breakdown tends to happen where the resistance is the highest rather than randomly according to the equation $Q = IR^2$, where Q, I, and R equal the Joule heat, current, and resistance, respectively, leaving the denser array less affected compared to the other array with a lower density. Figure S6 illustrates an example where the density of one array is four times that of the other and breakdown happens in the less dense array (Figure S6b), as expected, which is marked by the red circle. It should be emphasized that there is a chance that all breakdowns happen in one array and applications of bias cannot break the metallic pathways through s−m junctions. In our experiment, however, such an event is found to happen only when the density of the two crossing arrays differs significantly (for instance, one is more than twice of the other) as mentioned above due to the difference in resistance. Thus, to minimize the statistical probability for such an event, it is important that two crossing SWNT arrays with similar densities are used in our experiments so that the breakdown will happen randomly.

Comparison with Junction-Less Electrical Breakdown. Next, the effectiveness of the junction-based electrical breakdown is compared to that of directly applying a voltage across

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parallel nanotube arrays (namely, junction-less breakdown) under nongating conditions. Figure 3a shows a device with SWNT arrays directly bridging the two electrodes before and after breakdown. Similarly to the junction-based breakdown, defects can be observed after the process (marked by red circles). For the representative device, the current as a function of time was monitored, and the breakdown was terminated after current dropped to ~1/5 of the starting level (Figure 3b). Afterward, it is found that the on-state current of the device degrades to ~10% of the value before breakdown. The subthreshold curves before (dark brown) and after (red) the junction-less breakdown are given in Figure 3c. Current retentions of more test devices operated by the junction-less breakdown are plotted in Figure S7. The average value and median for the junction-less breakdown are 17% and 10%, which are in sharp contrast with the corresponding values of 49% and 44% for junction-based breakdown as mentioned above. Clearly, during the junction-less breakdown process, both m-SWNTs and a portion of s-SWNTs are damaged. Different current drop levels before stopping the junction-less breakdown process were also studied, but it is difficult to realize a general protocol that allows high on-state current retentions as well as high on/off ratios for all test devices simultaneously. This fact indicates the presence of floating threshold voltages of s-SWNTs probably caused by both the doping of molecules in the air and the surface charge trapping. According to the results, one can conclude that the junction-based breakdown amplifies the conductivity difference between s- and m-pathways under nongating conditions, leading to the highly selective scission of metallic pathways while preserving the transport properties of the s-SWNTs much better.

To compare the utility of our junction-based breakdown with the current state-of-the-art technique, we further conducted junction-less breakdown with gating, which has been commonly and widely used to purify SWNT arrays in previous studies.[28,46,47] Herein, a positive gate voltage (V_{GS} = 40 V) is applied to deplete charge carriers from s-SWNTs, and a bias voltage is added across the junction-less devices to allow stepwise drops of I_D in a way similar to the junction-based breakdown (Figure 3d, and see the method section in SI for details). Figure 3e shows the subthreshold curves of a representative gated junction-less device before (blue) and after (green) breakdown. The on/off ratio is increased from 8.3 to 7.5×10^4, and the current retention is 25%. Upon testing more devices, the median on/off ratio after gated junction-less breakdown is found to be 2.5×10^3, and the median and average value of current retention are 48% and 49%, respectively. Details on the on/off ratios and current retentions of all test devices are shown in Figure S8 in SI. The corresponding values for junction-based breakdown are 7.5×10^3, 44%, and 49%. For comparison, the box charts in Figure 3f summarize the distributions of current retentions of devices operated by the junction-based breakdown (green) and junction-less breakdown without (red) and with (black) gating. On the basis of the results stated above, it is believed that the efficiency and selectivity of our junction-based breakdown are comparable to those of the state-of-the-art approach, yet they can be achieved without a gate.

Mechanism of Amplification Effect in Junction-Based Breakdown. So far we have demonstrated the effective and selective breakdown of m-SWNTs based on nanotube junctions. To further investigate the breakdown mechanism, devices of junctions formed by crossbar of two individual nanotubes were fabricated and tested. Figure 4a shows the SEM image of a representative device, the configuration of which allows determination of the electrical properties of both the individual SWNTs and the junction. The behaviors of junction-less individual SWNTs during breakdown are first explored. Figure 4b shows the subthreshold curves of an s-SWNT and an m-SWNT, respectively. To have a better understanding on the breakdown current and voltage, the process is conducted by gradually ramping up V_{DS} until 80 V (V_{DS} beyond 80 V is not applied to avoid possible failures in the dielectrics). The breakdown curves of two SWNTs used in Figure 4b are shown in Figure 4c. The current of the m-SWNT increases almost linearly under low voltages, and then the slope decreases slightly, which is attributed to the increase of phonon scattering[48] before the m-SWNT is broken down at 13.9 V. For the s-SWNT, at the initial stage only a very low current is observed. After the voltage reaches ~7.5 V, however, the current increases rapidly, and the s-SWNT eventually breaks down at 36 V, which can be explained by the current injection caused by tunneling due to the avalanche effect.[49] Table S1 provides a collection of information on breakdown voltage and current of more individual SWNTs. It is found that all SWNTs can ultimately be broken down with the maximum breakdown voltage for m- and s-SWNTs being 18.7 and 66 V, respectively.

Similarly, devices based on junctions formed by two individual SWNTs are examined. Figure 4d shows the subthreshold curves of m−m (red), s−m (blue), and s−s (black) junctions, and the corresponding subthreshold curves of the junction-less SWNTs that form the three junctions are given in Figure S9. Note that the s−m junction carriers higher on-state current than the s−s junction, which can be attributed to the shorter channel length of s−SWNT via conduction through the m-SWNT. The junctions are subject to the same breakdown process as the individual SWNTs, and the I_D−V_{DS} curves are illustrated in Figure 4e. It is found that the m−m junction behaves entirely like an m-SWNT in the subthreshold curve with an on/off ratio of ~3.5. The current also increases linearly under applied V_{DS} in a way similar to m-SWNT and the breakdown voltage is 13.1 V, indicating that the resistance of the m−m junction is negligible. For the s−m junction and s−s junction shown in Figure 4d, both demonstrate semiconducting properties with a strong current modulation; however, for the output curves, the currents stay at relatively low levels that are not enough to break down a nanotube, and no drop is observed with V_{DS} all the way up to 80 V (for the s−s junction, the curve levels off at ~3×10^{-8} A, see Figure S10 in SI for details). More test device data is included in Table S1. It is observed that among all the s-SWNT-involved junctions, only 1/3 can be broken down under the same test conditions as that for the individual SWNTs, which is consistent with our hypothesis that the disparity between the resistance of s- and m-pathways is amplified in the junction crossbar structure. The results that the currents of s-SWNT-involving junctions saturate at relatively low levels and such junctions have a lower chance to be broken down compared with individual s-SWNTs support that the presence of junctions adds resistance to pathways involving s-SWNTs due to the Schottky barriers generated at the junctions. Consequently, the current output in s-pathways is suppressed, while that of m-pathways is not significantly affected because of the negligible m−m junction resistance, which enables selective breakdown upon the application of a bias voltage. Figure 4f illustrates an asymmetric transport behavior at an s−m junction under positive/negative bias that suggests a mismatch in work

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functions between the m- and s-SWNT, as schematically depicted in the corresponding band diagrams, which indicate the formations of Schottky barriers with different heights. It is believed that the height of the Schottky barrier plays an important role determining the carrier injection: when the barrier gets higher, it will be more difficult for carriers to tunnel through and therefore, the current in the corresponding s-pathway will be more obviously suppressed. It was reported that s-SWNTs with larger band gaps form higher Schottky barriers with metals (in our case m-SWNTs).[2] So generally, we believe factors (e.g., diameter of SWNT, surface adsorbates) that increase the band gaps of s-SWNTs will enhance the disparity between s- and m-pathways, and vice versa. On the other hand, we also point out that our method should work with similar efficiency and selectivity for SWNTs out of the present measurement range (0.93–2.87 nm) as long as the Schottky barrier is significant enough to distinguish s-pathways from m-counterparts. This study opens the way for further explorations of carrier transport behaviors at nanotube junctions.

In conclusion, a facile and effective approach is developed to selectively break down m-SWNTs by flowing currents into cross-stacked SWNT arrays without gating. The results show that m-SWNTs can be completely broken while most, if not all, s-SWNTs remain intact. Accordingly, FETs with high on/off ratios as well as high on-state current retentions can be obtained. This method enables the capability of selectively breaking down m-SWNTs in horizontally aligned array by adding voltage across SWNT junctions. In addition, the junction-based electrical breakdown is compared with the process that involves directly applying voltage across aligned SWNT arrays (junction-less breakdown), and it is further confirmed that the former is more selective and less damaging to the s-SWNTs. This method features the amplification of conductivity difference between s- and m-pathways by forming junctions. Even for a device requiring top gate/dielectrics, this approach can be applied if the junction-based breakdown is conducted before the deposition of the top layers. For instance, in thin-film nanotube devices on plastic or glass substrates where no back-gate is present, junction-based breakdown can be used to purify arrays prior to top gate fabrication. Finally, the mechanism of the amplification effect is carefully investigated by studying the breakdown behavior of three types of junctions created by individual SWNTs. It is believed that the formation of Schottky barriers in s-SWNT-involving junctions plays a significant role in suppressing the conductivity of s-pathways. Overall, this method provides a simple and promising way to obtain FET devices based on SWNT arrays with very high on/off ratios as well as opens the possibility for new discoveries regarding carrier transport through nanotube junctions.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b02261.

Detailed information on preparation of SWNT crossbars, SWNT characterization, transistor fabrication, electrical breakdown, and measurement along with supporting data (PDF)

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Notes

The authors declare no competing financial interest.

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