Vertical Carbon Nanotube Devices With Nanoscale Lengths Controlled Without Lithography

Aaron D. Franklin, Robert A. Sayer, Timothy D. Sands, *Senior Member, IEEE*, David B. Janes, *Member, IEEE*, and Timothy S. Fisher

***Abstract*—Vertical single-walled carbon nanotubes (v-SWCNTs) are synthesized within highly ordered porous anodic alumina (PAA) templates supported on Si substrates. A process for obtaining thin-film PAA with long-range ordered nanopores is presented in this paper. Each nanopore contains at most one v-SWCNT that is supported by a dielectric and addressed by electrochemically formed Pd nanowire source contacts and evaporated Pd drain contacts. Characteristics of these completely vertical, two-terminal nanotube devices are presented. Control of the v-SWCNT length is demonstrated using a straightforward etching process with lengths of less than 100 nm achieved without the need for complex/expensive lithography. This effective nanoscale length control of highly ordered v-SWCNTs provides a practical basis for the realization of CNT-based nanoelectronics.**

***Index Terms*—Carbon nanotubes (CNTs), length scaling, nanotechnology, porous anodic alumina (PAA), vertical devices.**

I. Introduction

THE UNIQUE properties of single-walled carbon nanotubes (SWCNTs), such as 1-D electrostatics and equal electron and hole effective masses, make them ideal for many nanoelectronic applications, from interconnects to FETs. With ballistic transport attainable and high current-carrying capacity, SWCNTs could enable the fastest and most robust electronics to date. However, as with most nanomaterials studied in the last decade, control of the placement and addressability of SWCNTs still precludes their integration in practical applications. Recent progress has been reported on the planar alignment of SWCNTs on a substrate via directed growth techniques [1]–[3], which offer improved control over the SWCNTs directionality; however, definition of the lateral density of the planar SWCNTs remains a challenge, with a best reported controlled density to date of ten SWCNTs per linear micrometer [2]. Also, as the SWCNTs become more densely packed, the spacing between them becomes less controlled [3], and the final devices can suffer from inhomogeneous charge screening effects between the SWCNTs [4], [5]. Furthermore, control of SWCNT length, which would serve as the channel length in a self-aligned FET, still requires advanced lithographic processes with high costs and low throughput that are not amenable to large-scale integration.

Nanoporous templates are becoming attractive for supporting nanomaterials, and improving their placement and addressability. These nanoporous templates can serve a variety of purposes from templating the synthesis of a nanomaterial [6], [7] to providing a support for *in situ* device fabrication [8]. The growth of SWCNTs from thin-film porous anodic alumina (PAA) templates has been recently achieved with a yield of not more than one SWCNT per pore [7], [9]. However, achieving highly ordered pores by anodization of Al requires several micrometers of Al and a two-step anodization process, as the initial nucleation of the pores is controlled by defects in the Al surface. The thicknesses of smooth Al films obtained by physical vapor deposition are generally insufficient to obtain the degree of pore order in PAA that is characteristic of PAA fabricated by two-step anodization of Al foil or bulk Al [10].

Herein, we present a new process for obtaining well-ordered thin-film PAA, which serves as the template for synthesizing completely vertical SWCNTs (v-SWCNTs). These self-aligned v-SWCNTs differ from previously reported SWCNTs in PAA [9] as these are completely vertical and confined to their nanopores without a lateral extension above the surface, and they have a potential density of 115 SWCNTs/μm^2 with an SWCNT–SWCNT spacing of 100 nm. Source and drain contacts are established using electrochemical and physical vapor deposition, respectively. The length of the v-SWCNTs is controlled using simple deposition and/or etching techniques with a variability of $\pm$10 nm over hundreds of devices—for the first time, nanoscale length SWCNT devices have been realized without the need for any lithographic patterning of the SWCNTs. For verification of the semiconducting nature of the SWCNTs synthesized from these PAA templates, planar FETs are fabricated that demonstrate modulation of the channel current over more than five orders of magnitude.

II. Device Fabrication

The process for obtaining highly ordered PAA thin films and subsequently synthesizing v-SWCNTs within the nanopores is shown in Fig. 1 with schematics and field emission SEMs. On an Si substrate, the following film stack is thermally evaporated: 100 nm Ti/100 nm Al/1 nm Fe/300 nm Al.

Manuscript received August 11, 2008; revised October 29, 2008. First published January 13, 2009; current version published July 9, 2009. This work was supported by the National Science Foundation Graduate Research Fellowship (A. D. F.). The review of this paper was arranged by Associate Editor J. Rogers.

A. D. Franklin and D. B. Janes are with the School of Electrical and Computer Engineering, and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: aaron-franklin@purdue.edu; janes@purdue.edu).

R. A. Sayer and T. S. Fisher are with the School of Mechanical Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: rsayer@purdue.edu; tsfisher@purdue.edu).

T. D. Sands is with the School of Materials Science Engineering, School of Electrical and Computer Engineering, and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: tsands@purdue.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2009.2012399

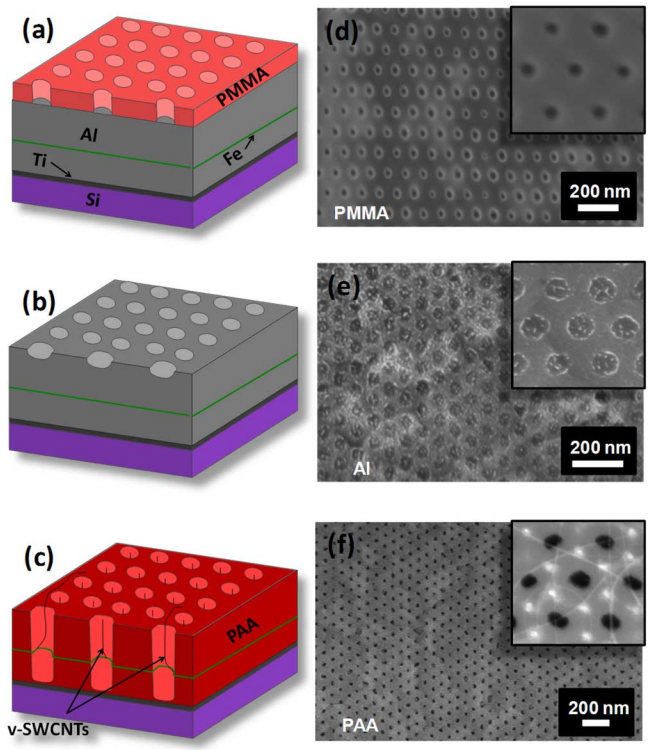

Fig. 1. Process for obtaining highly ordered v-SWCNTs. Schematics illustrating (a) the EBL patterning of PMMA with a hexagonal pattern of 100 nm spacing, (b) the Al surface following a brief wet etch to transfer the pattern, and (c) the PAA template formed by anodization with self-aligned v-SWCNTs synthesized from the embedded Fe layer. (d)–(f) Top-view SEMs of a sample at each step of the process. The inset SEM in (f) shows SWCNTs that have grown out of their respective nanopores and extend laterally on the PAA surface.

Polymethyl-methacrylate (PMMA) resist is then applied, and a hexagonally arranged pattern is exposed using electron beam lithography (EBL). Even though EBL is used for the demonstration herein, this redundant pattern can be produced at the wafer scale using nanoimprint or interference lithography, for example [11]. After development, the hexagonal pattern is transferred to the Al surface by a 25 s wet etch using Transene Al-etchant type A at room temperature with moderate agitation. The resulting pits in the Al surface [observed in Fig. 1(e)] serve as the nucleation sites for pore formation in an electrochemical anodization. In 0.3 M oxalic acid, the samples were anodized at 40 V until the current decreased from the range of several milliamperes to several microamperes, indicating the complete anodization of the Al layers to form PAA. Microwave plasma-enhanced chemical vapor deposition (MPCVD) was subsequently used to synthesize the SWCNTs [7], which nucleate at the embedded Fe layer within the pores and grow vertically to the PAA surface with a yield of not more than one SWCNT per pore, as reported previously [7], [9]. Note that the Fe catalyst used in this paper is thinner than in a previous study [7], and this catalyst is expected to predominantly yield single-walled nanotubes by decreasing the catalyst particle size [12]. The density of SWCNTs in the present templates was kept extremely low by growing for times of 1 min or less in order to facilitate the testing of single (or few) nanotube devices per 100 μm^2 contact area—prior study has shown the ability to increase the SWCNT density when needed [12]. The inset of Fig. 1(f) shows SWCNTs that have grown beyond the top of their nanopore and are extending along the PAA surface. The protruding portions of the SWCNTs are removed in a subsequent etch to leave only the vertical channels of v-SWCNTs within the nanopores.

The spacing between nanopores in the hexagonally arranged template is 100 nm, which yields a potential v-SWCNT density of 115 SWCNTs/μm^2. Source contacts to the v-SWCNTs were made by electrochemically depositing Pd nanowires within the PAA pore bottoms, as described previously [6], [13]. The standard deviation in the length of these nanowires has been reported to be 4% [6] or less than 10 nm in the present case. A spin-on glass (SOG) dielectric (Honeywell 214) was then applied at 6000 r/min for 30 s followed by a 450 °C cure in N_2 for 1 h to support each v-SWCNT within its respective pore. The SOG fills the pores, provides a passivating dielectric support of the v-SWCNTs, and forms a planar layer on the PAA surface that is ≈180 nm thick.

Removal of this surface SOG was accomplished using an inductively coupled plasma reactive ion etcher (ICP-RIE). An inert gas plasma was supported by 60 sccm Ar at 1 mtorr and 300 W of coil power, while the Ar ions were accelerated to the sample surface with an 800 W platen bias power. The resulting ion bombardment etch removes the 180 nm of surface SOG, along with the portions of the SWCNTs that extended along the PAA surface, in 80 s. Use of fluorine-based chemical etchants for removing the silicate-based SOG proved to etch the v-SWCNTs within the PAA, completely removing them. Thus, the inert gas ion bombardment etch is important for the protection of the v-SWCNTs while planarizing the template surface. Continued ion bombardment etching past 80 s removes the PAA/v-SWCNT template at a vertical rate of 40 nm/min as determined from 42 etching trials with different etching times. After the etch, the top of the SOG within the nanopores is relatively level with the PAA surface.

III. Control of Nanotube Length

Evaporation of 8 nm Pd/20 nm Ti/60 nm Au top contacts of various sizes completes the fabrication of the two-terminal devices. Fig. 2(a) illustrates the final SWCNT length (L_{CNT}) in these devices, which is defined from the top of the Pd nanowire source contact to the top of the PAA template. L_{CNT} has been controlled by a combination of the initial top Al layer thickness (300 nm in the present case) and the ion bombardment etch time on the PAA/v-SWCNT template. The accuracy of controlling L_{CNT} from device to device by the top Al thickness strongly depends on the uniformity of the Al film. Because these are thin films, common planarizing processes such as chemical mechanical polishing and electropolishing are not possible because they would require a much thicker Al layer. Therefore, the roughness of the Al film is determined solely by the deposition process, which was thermal evaporation in this case with a surface roughness around 40 nm, as determined from cross-sectional SEMs of the deposited film. Typically, even with the smoothest achievable Al surface, the control of the v-SWCNT length from device

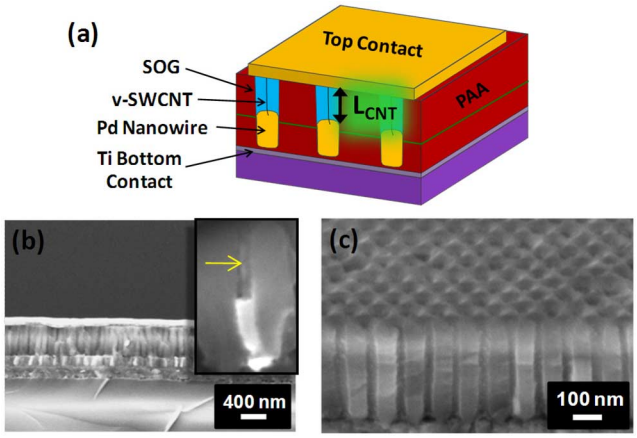

Fig. 2. (a) Schematic cross section of a two-terminal, multinanotube v-SWCNT device. (b) Cross-sectional SEM showing the vertical nanopores and Pd nanowire bottom contacts with a Pd/Ti/Au top contact. Inset shows a v-SWCNT supported in SOG with an arrow indicating the v-SWCNT location. (c) Tilted cross-sectional SEM showing the ordered nanopores prior to top contact metallization.

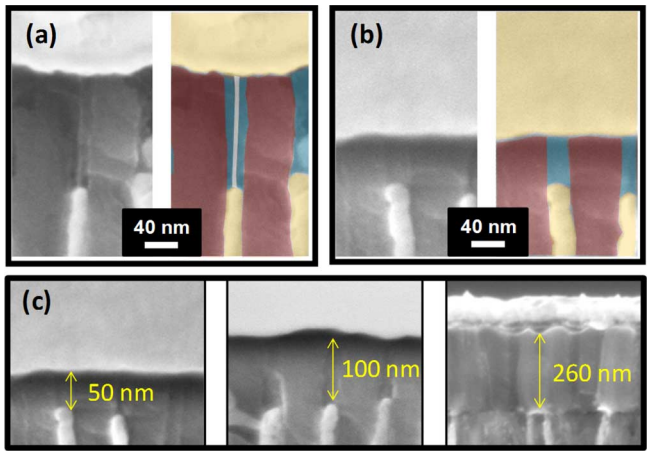

Fig. 3. Cross-sectional SEMs showing v-SWCNT lengths that have been controlled by using different ion bombardment etch times. Additionally, (a) and (b) show false color SEMs for material delineation (red is PAA, yellow is Pd, blue is SOG, and white line is v-SWCNT). (c) Arrows indicate the distance between the top of the Pd nanowire and the top of the PAA (or the beginning of the top contact). Note that fracturing the samples for SEM prep caused the Pd nanowires to break away from some pores.

to device will not be less than 30 nm because of the variation in etching the Al pits and the subsequent expansion of the film during transition from Al to alumina. However, control of the length from sample to sample by varying the initial Al thickness can be accomplished with reasonable accuracy as long as the expansion factor is taken into account.

The ion bombardment etch, however, yields very accurate control over the v-SWCNT length as compared to simply varying the Al thickness. Notably, the etch rate of the surface SOG (2.25 nm/s) is more than three times faster than the etch rate of the PAA/v-SWCNTs (0.67 nm/s). This rate difference enables close control in defining the v-SWCNT length. As seen in the SEM of Fig. 2(b), the final L_{CNT} is also affected by the uniformity of the Pd nanowire height, and the roughness of the initial substrate and underlying films. Taking these factors into consideration, the ion bombardment etch has produced nanoscale v-SWCNT lengths with a variability of ± 10 nm from device to device, as determined from cross-sectional SEMs over hundreds of devices. Fig. 3 shows cross-sectional SEMs of several different v-SWCNT device structures with lengths from 50 to 260 nm that have been defined using the ion bombardment etch for different durations. In the context of fabricating CNT FETs (CNTFETs), achieving a channel length between 50 and 70 nm should not produce substantial operational differences [14], [15], considering that the low-field transport at this length is ballistic in defect-free CNTs [16]. Also, it has been shown that channel lengths between 50 and 150 nm are optimal for CNTFETs (with top gates) to avoid short-channel effects while still maintaining ballistic transport [14], [15], [17].

IV. Results and Discussion

Electrical characteristics from a two-terminal v-SWCNT device consisting of one metallic and one semiconducting nanotube are shown in Fig. 4. The dimension of the top contact for

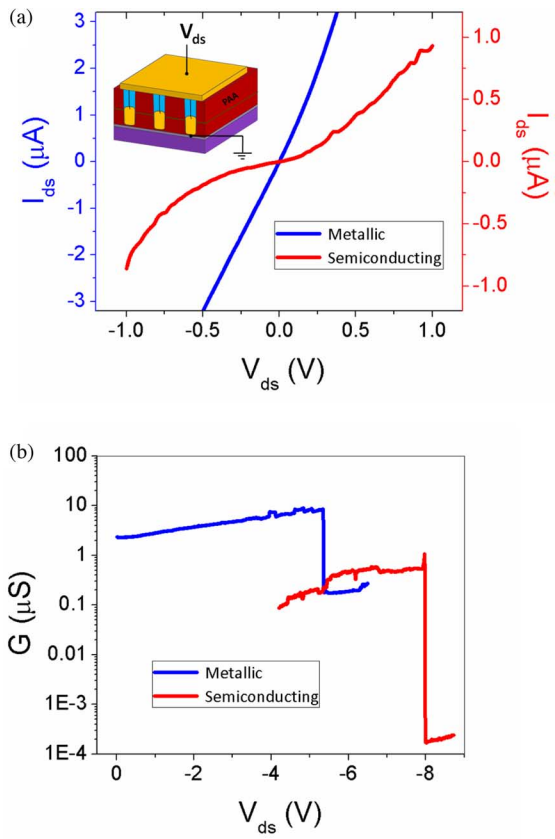

Fig. 4. (a) I–V characteristics from a two-terminal v-SWCNT device ($L_{\mathrm{CNT}} \approx 100$ nm) showing domination in conduction by a metallic v-SWCNT before it is burned out (blue) and by a semiconducting v-SWCNT after the metallic tube is burned (red). (b) Conductance versus applied bias showing the burn-out of the metallic v-SWCNT first (blue) and the subsequent burn-out of the semiconducting v-SWCNT (red).

all devices tested is 10 μm $\times$ 10 μm, which yielded between zero and two v-SWCNTs per device (the density of nanotubes was purposely kept low to achieve devices consisting of a single v-SWCNT). Initially, the device in Fig. 4 exhibits nearly symmetrical, linear I–V characteristics. When a high bias is swept, the conductance drops abruptly by over an order of magnitude corresponding to the breakdown (burn out) signature of a metallic tube as observed previously in planar devices [18], [19]. Importantly, the conductance does not drop to zero, but rather remains at a few tenths of a microSiemen. This conductance is attributed to the remaining semiconducting v-SWCNT as observed by the red I–V curve in Fig. 4(a) that was obtained after burn out of the metallic nanotube. The nonlinear behavior results from Schottky barriers (SBs) at the contacts to the semiconducting nanotube. While SBs are typically small for p-channel transport in Pd-contacted nanotubes, they can still be present [20]. Also, the slight asymmetry in this I–V characteristic suggests a disparity in the SB height between the two contacts [21] (examined in greater detail in relation to Fig. 6). A final high bias sweep burns out the semiconducting v-SWCNT, shown as the red curve in Fig. 4(b).

With a v-SWCNT length below 300 nm (close to the mean free path for acoustic phonon scattering) [16], [22], a defect-free, metallic nanotube should be ballistic and exhibit a low-bias conductance near the theoretical limit of $4e^2/h$ (154.8 μS) [23]. The substantially lower conductance observed here is attributed to the series and contact resistances in the device. Perhaps, the main contribution is the thin alumina barrier at the bottom of each nanopore in the PAA template [6], which would create a large series resistance between the Pd nanowire and the underlying Ti layer. The low conductance of the semiconducting v-SWCNT is attributed to the normally OFF nature of semiconducting nanotubes in terms of band positions under no gate bias [illustrated in Fig. 6(b)]. The same conductance range was observed in more than 60 other semiconducting v-SWCNT devices from several samples (see Fig. 5). Significantly, the conductance did not show strong dependence on the v-SWCNT length with the L_{CNT} below $\approx$300 nm. Devices with lengths in the range 50–260 nm were studied. Out of 94 devices tested, 78 contained at least one v-SWCNT, leaving 16 without any nanotubes. Furthermore, only four of the 78 devices contained any metallic nanotubes—the statistical yield based on the chiral vector is one-third metallic nanotubes from a CVD growth [24]. Therefore, this result suggests a possible selectivity toward semiconducting nanotubes and further implies a greater yield of single- versus double-walled nanotubes by employing a thinner catalyst layer than in previous studies [7]. The final eight devices contained more than one semiconducting nanotube—after the first nanotube burned out, the device retained some conductance. However, dielectric breakdown of the SOG occurred at around 10 V before the remaining nanotube(s) could be burned out and counted.

Fig. 6(a) displays the I–V characteristics of a single semiconducting v-SWCNT device. The orange curve was obtained using the top contact as the drain (normal configuration), while the purple curve was obtained with the contacts reversed. It is important to note that this semiconducting v-SWCNT is operat-

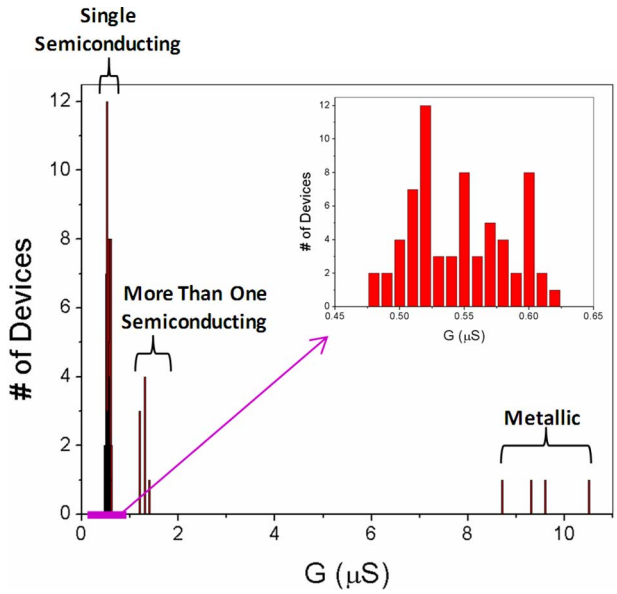

Fig. 5. Bar graph showing the number of devices that exhibited a certain conductance (rounded to the nearest hundredth of a microSiemen). The inset shows the distribution for the single semiconducting nanotube devices.

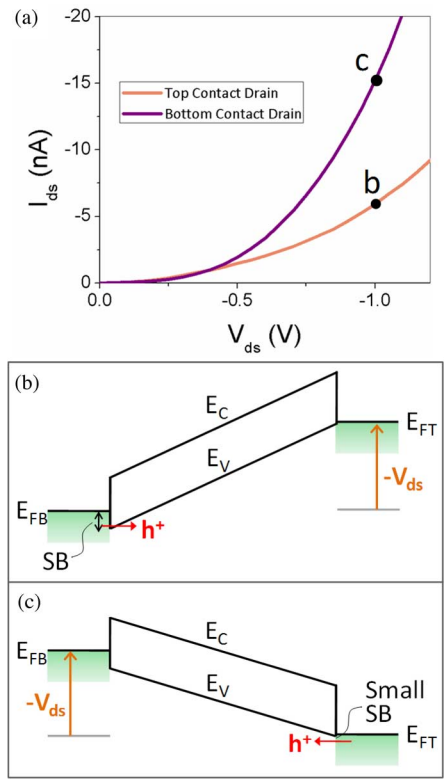

Fig. 6. (a) I–V characteristics from a single semiconducting v-SWCNT device with the contacts swapped (bias is applied to the top contact for the orange line and the bottom contact for the purple line). Qualitative band diagrams corresponding to (b) $V_{\mathrm{ds}} = -1$ V applied to the top contact and (c) $V_{\mathrm{ds}} = -1$ V applied to the bottom contact. The p-channel SB at the top contact is assumed to be smaller than the SB at the bottom contact for these illustrations. E_{FB} and E_{FT} denote the bottom and top contact metal Fermi levels, respectively.

ing in the OFF state; therefore, the hole current under the applied negative drain bias will be hindered in transporting from the source to the drain by the barrier in the bulk. Furthermore, the difference in current between this device and the semiconducting one in Fig. 4(a) is attributed to a variation in the band gap of the semiconducting nanotubes. The band gap is inversely proportional to nanotube diameter, and it is likely that the SWCNT diameters vary from device to device and within a given device. Smaller diameter nanotubes have larger band gaps, and correspondingly less conductance, especially because there is very little modulation of the thermal barrier in the channel of these devices (i.e., larger band gap devices exhibit lower current in the OFF state). Additionally, the larger band gap devices will have larger SBs, further reducing the current. Other variabilities, such as different alumina barrier thicknesses at the pore bottoms, could affect the series resistance and also alter the current.

The disparity between the two curves in Fig. 6(a) suggests a difference in the metal–SWCNT transport properties at the top and bottom contacts. The most obvious cause for such a contrast would be a disparity in the SB height at the contacts, which would cause a difference in current due to the exponential dependence of the current on the SB height [21], [25]. A factor that is likely contributing to the SB height difference is the use of electrodeposited Pd for the bottom contact, which may have a different work function than evaporated Pd. Because there is virtually no Fermi level pinning in metal–CNT contacts [26], this work function difference would produce a difference in SB height. In addition to the work function, the unique geometry of the contacts may also contribute to the disparity in current levels. For instance, the Pd nanowire bottom contact is formed around the v-SWCNT within the nanopore, which allows for transport to occur only between the metal and sidewalls of the nanotube. In contrast, the top contact is deposited directly to the tip of the v-SWCNT [see Fig. 2(a)], possibly enabling improved transport between the metal and the opened carbon bonds that were created during the ion bombardment etch. While the top contact may have a smaller overlap on the nanotube compared to the bottom contact, it has been suggested that the transport between a contact metal and SWCNT is dominated by the edge of the contacted region [27], but this opinion is not accepted universally. In fact, Knoch *et al.* have shown that both the metal work function and the metal–SWCNT coupling determine the transport properties at a metal–SWCNT junction [28]. A certain length of metal–SWCNT sidewall contact is necessary to obtain a desired coupling—too strong of a coupling could severely hamper the carrier transport. Thus, the short sidewall contact length exhibited in the present device may be causing a degradation of the current.

Qualitative band diagrams for a possible configuration of the semiconducting device are shown in Fig. 6(b) and (c) with operation under the two different contact configurations and the assumption that the SB at the bottom contact is substantially larger than the SB at the top contact. The absence of a gate on these fully depleted devices causes the screening length over which the potential will drop to be very large, resulting in an approximately linear drop of $V_{\rm ds}$ across the nanotube [28]. A $V_{\rm ds}$ of -1 V was chosen for comparison because it corresponds to a point at which the characteristics differ strongly with one another. When the drain bias is applied to the top contact, the hole current from the source is suppressed by the SB, requiring a substantial $V_{\rm ds}$ at the drain in order to sufficiently thin the barrier and allow for carriers to tunnel through. With the drain at the bottom contact, the smaller SB to the valence band on the source-end allows for holes to flow from the source more freely than in the prior configuration. This effect is evident both in the faster rise of the associated purple I–V in Fig. 6(a) and the larger resulting current at $V_{\rm ds} = -1$ V. Note that the SB to the conduction band in either configuration is large enough to be deemed insurmountable by electrons at the drain with low $V_{\rm ds}$.

These templated v-SWCNTs offer several benefits in nanoelectronic applications. First, the v-SWCNT length can be scaled down without the use of lithography. Variation of the ICP-RIE ion bombardment etch time (rate of 40 nm/min) provides good control over $L_{\rm CNT}$, which in the context of fabricating CNTFETs would serve as the device's channel length. Fig. 3 shows SEMs that demonstrate the scaling of $L_{\rm CNT}$ using the ion bombardment process. Additionally, the length scaling is accomplished for all devices on a chip in a single step compared to the typical use of EBL to write each individual device one at a time. Another benefit of the v-SWCNT structure is the ability to obtain individual channels of v-SWCNTs that are wrapped in a dielectric (SOG in this case). While SOG was used as a dielectric support for the nanotubes herein, the v-SWCNTs could alternatively be coated with a high-κ dielectric using atomic layer deposition (ALD) [29]. When fabricating multinanotube devices for interconnects or FETs, the individual channels of v-SWCNTs will minimize deleterious charge screening between nanotubes that other configurations encounter as the nanotubes become more closely packed and bundled [3]–[5]. In fact, the achievable density of nanotubes in the v-SWCNT templates is an order of magnitude greater than the best density reported to date for planar configurations—assuming a channel length of 100 nm and an additional loss of 1 $\mu{\rm m}^2$ for contact metallization in the planar geometry. Other benefits include the ability to use these v-SWCNT templates for fabricating surround-gated vertical CNTFETs [30], [31], creating ordered arrays of v-SWCNTs of adjustable density, or even using the v-SWCNT tips as probes for biological interfacing [32]. A recent modeling study [31] has shown that the presence of a gate underlap (which would be difficult to avoid in a vertical CNTFET geometry) actually suppresses ambipolar conduction and enables I–V characteristics better suited for digital applications.

To provide additional verification of the presence of semiconducting nanotubes in the v-SWCNT templates, planar CNTFETs were fabricated from the nanotubes. On the Si support substrate used for this portion of the study, each field of PAA was surrounded by a region of 200-nm-thick SiO_2 using a process reported previously [33]. In this case, the SWCNTs were grown for a longer time (15 min as opposed to 1 min for low density growth), which caused them to extend out of their pores and along the PAA surface [see Fig. 7(a)], and eventually over the SiO_2 regions. Finally, Pd source and drain contacts were

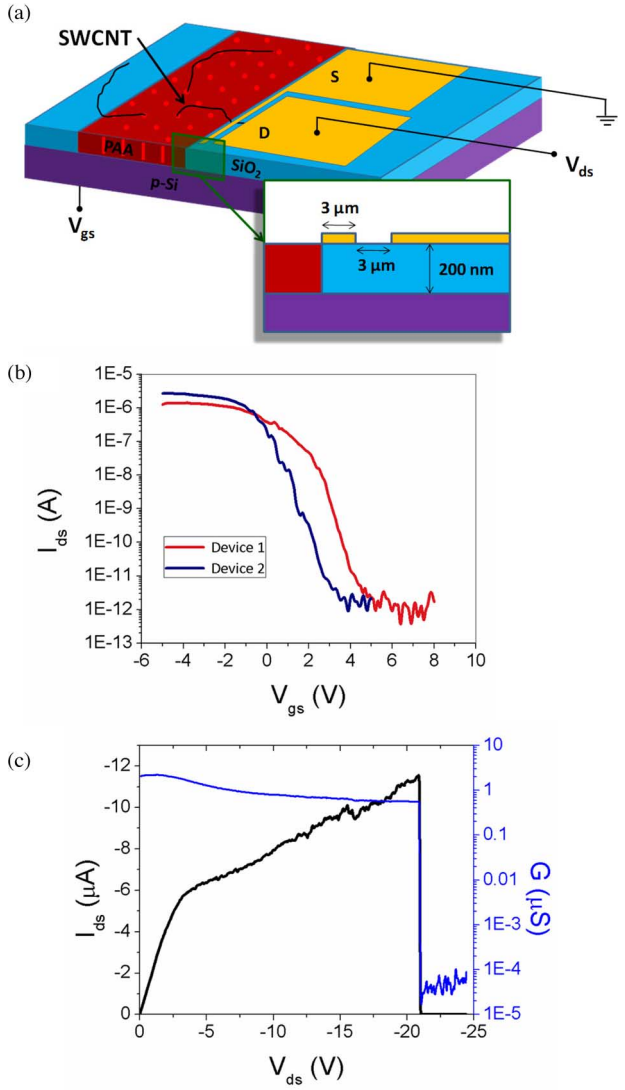

Fig. 7. (a) Schematic of planar CNTFETs fabricated from v-SWCNTs that have been overgrown from the PAA onto a neighboring oxide and contacted with Pd source/drain contacts. The gate dielectric is 200 nm of thermal SiO_2 with a 3 μm channel length. (b) Subthreshold characteristics of two representative devices, each containing a single semiconducting nanotube and displaying an I_{ON}/I_{OFF} current ratio of more than five orders of magnitude with $V_{ds} = -1$ V. (c) I–V and G–V characteristics showing the burnout of a single nanotube from one of the devices in (b) at $V_{gs} = -5$ V.

lithographically defined to contact the SWCNTs on the SiO_2 surface. The Si substrate was used as a back gate during measurement, as illustrated in Fig. 7(a). The final devices contained long channels (3 μm), which caused them to operate in the diffusive transport regime. However, these devices were sufficient for identifying the semiconducting nature of the SWCNTs by use of the back gate. Fig. 7(b) shows the subthreshold characteristics from two representative devices, which exhibit an I_{ON}/I_{OFF} ratio of over five orders of magnitude. The divergence in threshold voltage between the two devices is partially attributed to the lack of passivation, which has been noted in the past to cause a shift in threshold [34]. Note that the threshold for these devices will be different from the completely vertical SWCNT devices where the SWCNTs are supported in (and thus passivated by) a dielectric. We also note that the device geometries of this and the vertical two-terminal devices discussed before are different enough to preclude a quantitative comparison of their electrical characteristics; however, it is interesting that the current levels at $V_{gs} = 0$ V and $V_{ds} = -1$ V are quite comparable between the single semiconducting nanotube devices in Figs. 4(a) and 7(b). In the rare case that a metallic nanotube was present in these planar CNTFETs (only one out of 30 devices tested contained any metallic SWCNTs), the current changed less than one order of magnitude under the same applied gate bias. Furthermore, biasing the semiconducting nanotubes into the OFF state allowed for the selective breakdown of the metallic nanotubes with a high bias sweep [19].

V. Conclusion

Bringing SWCNTs closer to large-scale integration requires greater control over their placement and properties. These self-aligned arrays of v-SWCNTs templated in highly ordered PAA provide a simple and robust platform that could provide a basis for realizing practical SWCNT nanoelectronics. A new method for producing thin-film PAA templates with long-range ordered nanopores at a spacing of 100 nm has been presented. Each nanopore serves as a v-SWCNT channel containing a single SWCNT that is individually wrapped in a dielectric to minimize charge screening from other nearby SWCNTs. The ability to control the length of the v-SWCNTs (lengths between 50 and 260 nm were demonstrated) using a standard RIE etch process suggests a path toward manufacturing aggressively scaled CNTFETs that do not require advanced, expensive, and low-throughput lithography to define nanoscale channel lengths. Furthermore, these templates of v-SWCNTs provide a platform for fabricating surround-gated CNTFETs, which would have ideal gating electrostatics [17] for optimal transistor performance.

Acknowledgment

The authors gratefully acknowledge Prof. J. Appenzeller for stimulating discussions.

References

[1] S. J. Kang, C. Kocabas, H. S. Kim, O. Cao, M. A. Meitl, D. Y. Khang, and J. A. Rogers, "Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic, applications," *Nano Lett.*, vol. 7, pp. 3343–3348, 2007.

[2] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nat. Nanotechnol.*, vol. 2, pp. 230–236, 2007.

[3] C. Kocabas, S. J. Kang, T. Ozel, M. Shim, and J. A. Rogers, "Improved synthesis of aligned arrays of single-walled carbon nanotubes and their implementation in thin film type transistors," *J. Phys. Chem. C*, vol. 111, pp. 17 879–17 886, 2007.

[4] D. Jie, L. Albert, C. W. Gordon, and H. S. P. Wong, "Carbon nanotube transistor compact model for circuit design and performance optimization," *J. Emerging Technol. Comput. Syst.*, vol. 4, pp. 1–20, 2008.

[5] X. F. Li, K. Q. Chen, L. L. Wang, M. Q. Long, B. S. Zou, and Z. Shuai, "Effect of intertube interaction on the transport properties of a carbon double-nanotube device," *J. Appl. Phys.*, vol. 101, pp. 064 514-1–064 514-4, Mar. 2007.

[6] A. D. Franklin, M. R. Maschmann, M. DaSilva, D. B. Janes, T. S. Fisher, and T. D. Sands, "In-place fabrication of nanowire electrode arrays for vertical nanoelectronics on Si substrates," *J. Vac. Sci. Technol. B, Microelectron.*, vol. 25, pp. 343–347, Mar./Apr. 2007.
[7] M. R. Maschmann, A. D. Franklin, P. B. Amama, D. N. Zakharov, E. A. Stach, T. D. Sands, and T. S. Fisher, "Vertical single- and double-walled carbon nanotubes grown from modified porous anodic alumina templates," *Nanotechnology*, vol. 17, pp. 3925–3929, Aug. 2006.
[8] J. F. Dayen, A. Rumyantseva, C. Ciornei, T. L. Wade, J. E. Wegrowe, D. Pribat, and C. S. Cojocaru, "Electronic transport of silicon nanowires grown in porous $\mathrm{Al_2O_3}$ membrane," *Appl. Phys. Lett.*, vol. 90, pp. 173 110-1–173 110-3, Apr. 2007.
[9] M. R. Maschmann, A. D. Franklin, A. Scott, D. B. Janes, T. D. Sands, and T. S. Fisher, "Lithography-free in situ Pd contacts to templated single-walled carbon nanotubes," *Nano Lett.*, vol. 6, pp. 2712–2717, Dec. 2006.
[10] H. Masuda, F. Hasegwa, and S. Ono, "Self-ordering of cell arrangement of anodic porous alumina formed in sulfuric acid solution," *J. Electrochem. Soc.*, vol. 144, pp. L127–L130, May 1997.
[11] M. D. Austin, H. Ge, W. Wu, M. Li, Z. Yu, D. Wasserman, S. A. Lyon, and S. Y. Chou, "Fabrication of 5 nm linewidth and 14 nm pitch features by nanoimprint lithography," *Appl. Phys. Lett.*, vol. 84, pp. 5299–5301, 2004.
[12] M. R. Maschmann, A. D. Franklin, T. D. Sands, and T. S. Fisher, "Optimization of carbon nanotube synthesis from porous anodic Al-Fe-Al templates," *Carbon*, vol. 45, pp. 2290–2296, 2007.
[13] A. D. Franklin, J. T. Smith, T. Sands, T. S. Fisher, K. S. Choi, and D. B. Janes, "Controlled decoration of single-walled carbon nanotubes with Pd nanocubes," *J. Phys. Chem. C*, vol. 111, pp. 13 756–13 762, 2007.
[14] Y. M. Lin, J. Appenzeller, Z. H. Chen, Z. G. Chen, H. M. Cheng, and P. Avouris, "High-performance dual-gate carbon nanotube FETs with 40-nm gate length," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 823–825, Nov. 2005.
[15] R. V. Seidel, A. P. Graham, J. Kretz, B. Rajasekharan, G. S. Duesberg, M. Liebau, E. Unger, F. Kreupl, and W. Hoenlein, "Sub-20 nm short channel carbon nanotube transistors," *Nano Lett.*, vol. 5, pp. 147–150, Jan. 2005.
[16] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654–657, Aug. 2003.
[17] J. Appenzeller, "Carbon nanotubes for high-performance electronics—Progress and prospect," *Proc. IEEE*, vol. 96, no. 2, pp. 201–211, 2008.
[18] P. C. Collins, M. S. Arnold, and P. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," *Science*, vol. 292, pp. 706–709, Apr. 2001.
[19] R. Seidel, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Steinhoegl, F. Kreupl, and W. Hoenlein, "High-current nanotube transistors," *Nano Lett.*, vol. 4, pp. 831–834, May 2004.
[20] Z. H. Chen, J. Appenzeller, J. Knoch, Y. M. Lin, and P. Avouris, "The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," *Nano Lett.*, vol. 5, pp. 1497–1502, Jul. 2005.
[21] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and P. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Phys. Rev. Lett.*, vol. 89, pp. 126 801.1–126 801.4, Sep. 2002.
[22] A. Javey, J. Guo, M. Paulsson, Q. Wang, D. Mann, M. Lundstrom, and H. J. Dai, "High-field quasiballistic transport in short carbon nanotubes," *Phys. Rev. Lett.*, vol. 92, pp. 106 804-1–106 804-4, Mar. 2004.
[23] S. Datta, *Quantum Transport: Atom to Transistor*, 1st ed. Cambridge, U.K.: Cambridge Univ. Press, 2005.
[24] M. D. Dresselhaus, G. Dresselhaus, and P. Avouris, *Carbon Nanotubes: Synthesis, Structure, Properties and Applications*, 1st ed. Berlin, Germany: Springer-Verlag, 2001.
[25] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. J. Wind, and P. Avouris, "Carbon nanotube electronics," *IEEE Trans. Nanotechnol.*, vol. 1, no. 4, pp. 184–189, Dec. 2002.
[26] F. Léonard and J. Tersoff, "Role of Fermi-level pinning in nanotube Schottky diodes," *Phys. Rev. Lett.*, vol. 84, pp. 4693–4696, 2000.
[27] D. Mann, A. Javey, J. Kong, Q. Wang, and H. J. Dai, "Ballistic transport in metallic nanotubes with reliable Pd ohmic contacts," *Nano Lett.*, vol. 3, pp. 1541–1544, Nov. 2003.
[28] J. Knoch and J. Appenzeller, "Tunneling phenomena in carbon nanotube field-effect transistors," *Phys. Status Solidi A*, vol. 205, pp. 679–694, Apr. 2008.
[29] D. B. Farmer and R. G. Gordon, "Atomic layer deposition on suspended single-walled carbon nanotubes via gas-phase noncovalent functionalization," *Nano Lett.*, vol. 6, pp. 699–703, Apr. 2006.
[30] Z. H. Chen, D. Farmer, S. Xu, R. Gordon, P. Avouris, and J. Appenzeller, "Externally assembled gate-all-around carbon nanotube field-effect transistor," *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 183–185, Feb. 2008.
[31] Y. Yoon, J. Fodor, and J. Guo, "A computational study of vertical partial-gate carbon-nanotube FETs," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 283–288, Jan. 2008.
[32] K. S. Yum, H. N. Cho, H. Hu, and M. F. Yu, "Individual nanotube-based needle nanoprobes for electrochemical studies in picoliter microenvironments," *ACS Nano*, vol. 1, pp. 440–448, Dec. 2007.
[33] A. D. Franklin, D. B. Janes, J. C. Claussen, T. S. Fisher, and T. D. Sands, "Independently addressable fields of porous anodic alumina embedded in $\mathrm{SiO[sub\ 2]}$ on Si," *Appl. Phys. Lett.*, vol. 92, pp. 013 122-1–013 122-3, 2008.
[34] L. Rispal, T. Tschischke, H. Yang, and U. Schwalke, "Polymethyl methacrylate passivation of carbon nanotube field-effect transistors: Novel self-aligned process and effect on device transfer characteristic hysteresis," *Jpn. J. Appl. Phys.*, vol. 47, pp. 3287–3291, 2008.

Aaron D. Franklin received the B.S. degree in electrical engineering from Arizona State University, Tempe, in 2004. He is currently working toward the Ph.D. degree in electrical engineering in the School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN.

During 2004, he was a Research Intern at Purdue, where he was engaged in the synthesis of single-walled carbon nanotubes using plasma-enhanced chemical vapor deposition. From 2004 to 2005, he was a Component Design Engineer with Intel Corporation. His current research interests include manufacturability of carbon nanotube nanoelectronics with specific emphasis on vertical nanotube field-effect transistors with surround gating.

Mr. Franklin was the recipient of the 2005 National Science Foundation Graduate Research Fellowship Award.

Robert A. Sayer received the B.S. degree in mechanical engineering from Ohio State University, Columbus, in 2006. He is currently working toward the Ph.D. degree in mechanical engineering in the School of Mechanical Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN.

He was a Research Intern at Battelle Memorial Institute, Columbus, OH, from 2004 to 2005, and an undergraduate researcher in the Nanotribology Laboratory for Information Storage and Microelectromechanical Systems (MEMS)/Nanoelectromechanical Systems (NEMS) (NLIM), Ohio State University, from 2005 to 2006. His current research interests include electrical shot noise measurements of carbon nanotube devices.

Timothy D. Sands (M'02–SM'08) received the Ph.D. degree in materials science from the University of California, Berkeley, in 1984.

He was as a Member of Technical Staff and a Research Group Director at Bell Communications Research, Inc. (Bellcore), Red Bank, NJ, for nine years. Then, he joined the Department of Materials Science and Engineering, University of California. During 2001, he was a Visiting Professor at the Interuniversity Microelectronics Center (IMEC) and Faculty of Engineering, Katholieke Universiteit Leuven, Leuven, Belgium. In 2002, he became the Basil S. Turner Professor of Engineering at Purdue University, West Lafayette, IN, with a joint appointment in the Schools of Materials Science Engineering and the School of Electrical and Computer Engineering, where in November 2006, he became the Mary Jo and Robert L. Kirk Director of Birck Nanotechnology Center, Purdue's Discovery Park. He is the author or coauthor of more than 230 papers. He is the holder of 13 patents in the areas of metal/semiconductor contacts, heteroepitaxy, thermoelectric materials, ferroelectric and piezoelectric materials and devices, semiconductor nanostructures, laser processing, and heterogeneous integration. He is the coinventor of the excimer laser lift-off process for separation of GaN from sapphire, a process that is widely used world-wide in the manufacture of high performance blue and green LEDs. His current research interests include the development of novel nanocomposite materials for applications in solid-state lighting, direct conversion of heat to electrical power, and thermoelectric refrigeration.

Prof. Sands was the 1994 Fall Materials Research Society (MRS) Meeting Co-Chair (1994), and the Chair of the Electronic Materials Committee (EMC/TMS; 1995–97), University of California.

David B. Janes (S'86–M'89) received the B.A. degree in physics from Augustana College, Rock Island, IL, in 1980, and the B.S.E.E., M.S.E.E., and Ph.D. degrees from the University of Illinois at Urbana-Champaign, Urbana-Champaign, in 1980, 1981, and 1989, respectively.

From 1981 to 1985, he was a Research Scientist at the Research Division of Raytheon Company, where he was engaged in research on microwave devices and ICs. His doctoral research was focused on the impact of electron traps on the microwave performance of GaAs-based signal processing devices (acoustic charge transport devices). Since 1989, he has been at Purdue University, West Lafayette, IN, where he was the Research Program Coordinator for the Birck Nanotechnology Center from 2001 to 2003, and is currently a Professor of electrical and computer engineering. From 2003 to 2007, he was the Technical Director of the Institute for Nanoelectronics and Computing, a National Aeronautics and Space Administration (NASA)-supported center. His past research interests include experimental studies on mesoscopic devices and compound semiconductor microwave devices, and characterization of novel semiconductor heterostructures, including structures incorporating low-temperature-grown GaAs. His current research interests include the development of molecular electronic components, nanowire/nanotube transistors, and chemical sensors.

Timothy S. Fisher received the B.S. and Ph.D. degrees in mechanical engineering from Cornell University, Ithaca, NY, in 1998 and 1991, respectively.

He was at Vanderbilt University for several years. From 1991 to 1993, he was a Design Engineer in Motorola's Automotive and Industrial Electronics Group. In 2002, he joined the School of Mechanical Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN. His current research interests include efforts in simulation and measurement of nanoscale heat transfer, coupled electro-thermal effects in semiconductor devices, nanoscale direct energy conversion, molecular electronics, microfluidic devices, hydrogen storage, and computational methods ranging from atomistic to continuum scales. Applications of his work cover a broad range of areas, including nanoelectronics, thermal interface materials, thermal-electrical energy conversion, biosensors, and hydrogen storage.

Dr. Fisher is a member of the Tau Beta Pi and Pi Tau Sigma honor societies. He is a member of the IEEE Technical Committee (TC)-9 Committee on Thermal Phenomena in Electronics, the American Society of Mechanical Engineers (ASME) K-6 Committee on Heat Transfer in Energy Systems, and the ASME K-16 Committee on Thermal Management of Electronics.