Contacting and Gating 2-D Nanomaterials

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(Invited Paper)

***Abstract*— Two-dimensional (2-D) nanomaterials provide opportunities for a wide range of applications. In order to harness their usefulness, understanding and controlling the interface between 2-D crystals and other materials is of paramount importance. For electronic device applications, large contact resistance and difficulty integrating high-quality dielectrics are the most pressing challenges. In this review, we describe the progress and core challenges of various contact and gate engineering approaches in order to guide the direction of future research toward fabricating useful devices based on 2-D nanomaterials.**

***Index Terms*— 2-D, atomic layer deposition (ALD), carrier injection, contact resistance, field-effect transistor (FET), molybdenum disulfide (MoS_2), plasma-enhanced ALD (PEALD).**

I. Introduction

OVER the past decade, atomically thin, 2-D nanomaterials have become an active platform for investigating a wide range of novel physical phenomena and applications [1], [2]. Starting with graphene, new 2-D nanomaterials with diverse properties continue to emerge, from insulator to metallic, and from elemental to compound [3]. Applications based on 2-D nanomaterials are as expansive as the variety of materials themselves, including electronics, energy storage, photonics, and sensors. The ultrathin nature of semiconducting 2-D crystals offers particular promise for future scaled electronic devices. While considerable progress has been made in scaled high-performance 2-D transistors [4]–[8], significant challenges remain related to interfaces with the 2-D crystals in these devices. The 2-D surface (basal) plane has no dangling bonds, making contact metal and gate dielectric interfacing unique and challenging, as illustrated in Fig. 1.

Among the 2-D crystal options, semiconducting transition-metal dichalcogenides (TMDs) have attracted most of the attention for electronic devices, with additional consideration of so-called X-enes (e.g., silicene [9], germanene [10], phosphorene or black phosphorous (BP) [11], and for some applications, graphene [12]). There have been several review papers comprehensively covering aspects of contact engineering to these various 2-D nanomaterials [13]–[18]. In this review, we focus on the core challenges of the 2-D nanomaterial interfaces (for both contacting as well as gating) and identify key questions and objectives to guide further research. We first cover contact geometries, the contact interface, and the largely neglected contact scaling issue, which is of utmost importance for 2-D devices given the motivation for using them at scaled dimensions. After proposing a holistic view to assess contact engineering approaches, we turn to gate engineering. A typical process of growing dielectrics using atomic layer deposition (ALD) is introduced. Then, we discuss different approaches for improving the gate dielectric quality, including surface treatment, buffer layers, and ALD process modification.

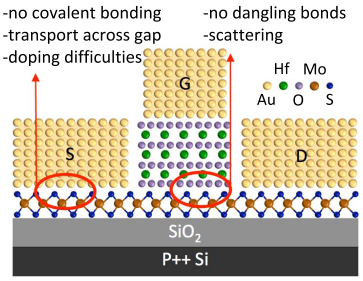

Fig. 1. Schematic overview of challenges for contact and gate interfaces in a typical 2-D FET with MoS_2 channel, Au contacts, and HfO_2 gate dielectric.

II. Contacts to 2-D FETs

The contact interface for 2-D field-effect transistors (FETs) typically involves a 3-D contact on the top of the 2-D nanomaterial, as illustrated in Fig. 2(a) with molybdenum disulfide (MoS_2) as an example. Although the physics of interfacial interactions and carrier injection mechanisms are not fully understood, it is generally believed that electrons first tunnel through the van der Waals gap between the metal contacts and the 2-D nanomaterial, depicted as the red arrows in Fig. 2(a) and (b) [14]. Then, the injected electrons from the source contact flow to the drain under an electric field from V_{ds}. Transistors benefit most from output curves (I_d–V_{ds}) with features like those in Fig. 2(c). According to the final (2015) ITRS roadmap [19], a device for low-power applications around 2030 has to sustain sufficient ON-current (I_{ON} = 1500 μA/μm) and operate at a low supply voltage of $V_{dd} \leq$ 0.5 V with ohmic contacts and a small contact resistance.

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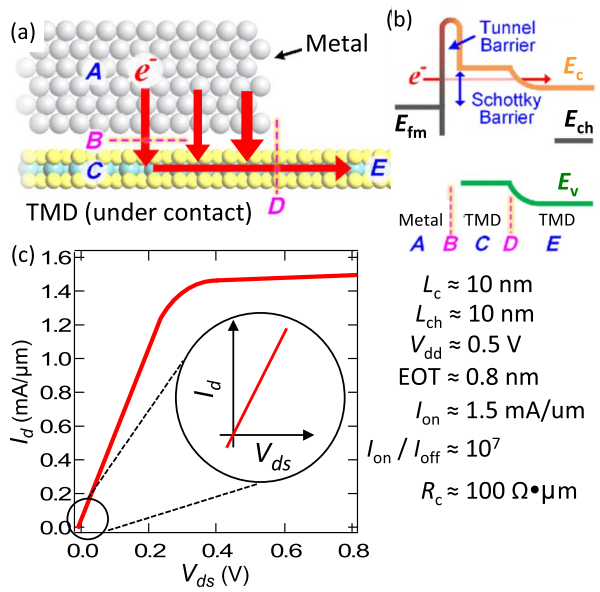

Fig. 2. Overview of transport at the contacts at a typical metal-2-D interface. (a) Simplified and cross-sectional diagram of carrier injection. (b) Band diagram of the interface assuming a weak bonding between the contact and the TMDs. (c) Example of the desired output curves and parameters for an n-type 2-D FET in the 2030 era [19]. (a) and (b) Reprinted from [46].

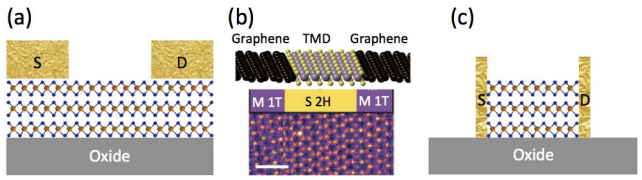

Fig. 3. Three different contact geometries. (a) Metal top contacts where the contact rests on the top of the 2-D nanomaterial. (b) In-plane 2-D contacts, including graphene and metallic 1T TMDs, adapted with permission from [38] and [42], respectively. (c) Metal edge contacts.

A. Contact Geometries and Materials

There are primarily three different contact geometries that have been explored for 2-D FETs: top contacts, in-plane 2-D contacts, and edge contacts. The vast majority of studies use the top contacts due to the simplicity of fabrication. As shown in Fig. 3(a), 3-D metal top contacts rest on the top of the 2-D nanomaterial. Approaches for improving the 2-D FET performance with the top contacts include using different contact metals [6], [7] [20], [21], annealing [22], [23], adding an interlayer at the contact interface [24]–[28], engineering surface states [29], and doping chemically [30]–[33] or physically [34].

The second type of contact geometry uses 2-D nanomaterials, such as graphene, to form an in-plane contact interface [Fig. 3(b)]. For example, the interaction between MoS_2 and graphene has exhibited ohmic contact behavior [35]–[40]. Note that an "ohmic contact" does not guarantee small contact resistance as linear output curves (at small V_{ds}) could have a small slope, and thus a large contact resistance. Some 2-D crystals, such as MoS_2, exhibit both semiconducting and metallic phases, enabling the use of the metallic phase to create an in-plane 2-D contact [41]. Note that this phase engineering requires high-processing temperature of 600 °C [42] and thus is not compatible with the traditional semiconductor fabrication processing. Electrostatic doping has also been reported to induce the structural phase transition in monolayer $MoTe_2$ [43]; however, more work is needed to implement fabrication-friendly phase engineering that yields better contacts.

Finally, edge contacts [Fig. 3 (c)] to 2-D nanomaterials have been demonstrated [8], [44], [45]. The most notable example uses a chromium (Cr) edge contact to graphene that yields contact resistance as low as 150 $\Omega \cdot \mu$m [8]. While edge contacts to MoS_2 have received limited investigation, molecular dynamic simulation for the metal-MoS_2 edge contacts suggest they can outperform top contacts due to more intimate orbital overlapping between the metal atoms and edge states of MoS_2 [46]. Yet, despite such promise, experimental realizations of edge contacts show small ON-currents, possibly due to the sensitive MoS_2 edge states and small contact area exposed on the edge [44], [45]. The possibility of a more efficient contact between the MoS_2 edge and metal is intriguing and requires more in-depth research. In Section II-D, recent results on the advantageous scalability of edge contacts will be discussed.

B. Contact Interface

Understanding the contact interface is pivotal for improving carrier transport. Here, we discuss two important questions that warrant further research.

Is interfacial reaction helpful or harmful? Some metals, such as Ti, have been found to form compounds with S in MoS_2 in the top contact geometry [47], [48]. The Ti_xS_y compound was formed under ultra-high vacuum conditions, as confirmed by X-ray photoelectron spectroscopy (XPS) [Fig. 4(a)]. The covalent bonds between metal and MoS_2 are likely due to S vacancies present on the MoS_2 surface. However, the formation of these bonds does not guarantee superior performance, as Ti still forms a worse contact than Cr and other high work function metals such as Au and Ni [49]. Another contact interface challenge is the manifestation of a Fermi-level pinning-like behavior, as shown in Fig. 4(b) [50]. Density functional theory simulations suggest the Fermi pinning is a result of interfacial interactions, where the metal work function can be modulated by interface dipoles due to charge redistribution [51]. A recent study [Fig. 4(c)] on transferred metal demonstrates a substantially quenched Fermi-level pinning effect, attributed to the pure van der Waals interface produced by the transferred metal approach [52]. The study also suggested that the commonly used metal evaporation approach promotes a metal-2-D interfacial interaction (via damage to the 2-D crystal), leading to a strong Fermi-level pinning effect.

On the other hand, according to some theoretical simulations, different bonding strengths and orbital overlapping between metals and 2-D materials could lead to a small Schottky barrier and thus high carrier injection efficiency [46], [53]–[55]. Many experimental studies intentionally add defects to the contact region to promote more covalent bonds and interfacial reactions at the metal-2-D interface and

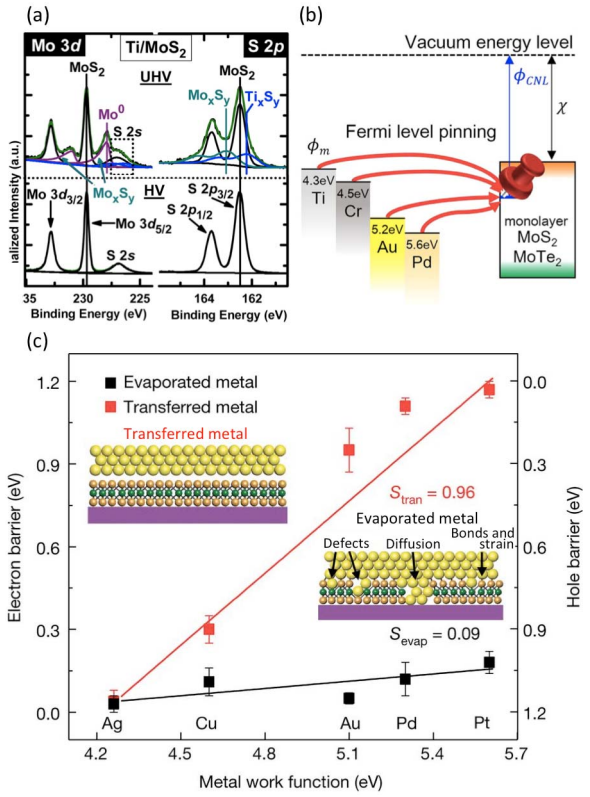

Fig. 4. Understanding the contact interface. (a) XPS characterization of interface chemistry of Ti on MoS_2 showing hybridization and covalent bonds at the interface. Adapted from [47] with permission. Copyright 2016 American Chemical Society. (b) Illustration of Fermi-level pinning at the metal-2-D interface. Adapted from [50]. Copyright 2017 American Chemical Society. (c) Comparison of evaporated metal and transferred metal showing strong Fermi-level pinning effect for the evaporated metal and obedience to the Schottky–Mott law for the transferred metal. Adapted from [52] with permission. Copyright 2018 Springer Nature.

do observe improvement in the contact performance [56]–[58]. The proposed mechanism for these experimental observations typically involves: creation of defects → more metal-2-D bonds → smaller (or thinner) Schottky barriers → smaller R_c. However, there are many open questions remaining to be answered, such as how high the suitable defect density is and how metal-2-D bonds impact the Schottky barrier. Thus, there has yet to be a comprehensive picture that captures exactly how interfacial interactions impact the carrier injection, and thus, further studies are needed.

How does contact gating and 2-D nanomaterial thickness influence the transfer length? The back-gate geometry (typically using a doped Si substrate as the gate electrode) is the most commonly used gating approach in 2-D FETs due to the ease of fabrication. In a back-gated device, the metal-2-D interface will be modulated by the back gate, creating a contact gating scenario. Contact gating has been examined in the past, and the transfer length (L_T) was extracted to be ~0.63 μm for monolayer devices using $L_T = (\rho_c/R_{sh})^{1/2}$, in which ρ_c is the metal-2-D interfacial resistance and R_{sh} is the lateral sheet resistance of the 2-D material underneath the metal contact [59]. However, more recently, a two-path carrier injection model has been applied by [60] and [61], both of which suggest a much smaller L_T for back-gated monolayer 2-D devices. In the two-path model, path 1 represents carrier injection from the metal to the edge of the 2-D channel, and path 2 accounts for carriers vertically tunneling to the metal-covered 2-D crystal and then laterally traveling to the channel region. The back-gate modulation of the metal-2-D interface allows for even more carriers in path 2, which explains why back-gated geometries outperform top-gated geometries with the same monolayer [62] and seven layers [59] 2-D channels.

Even when using the same gate geometry, 2-D nanomaterial thickness (number of layers) can also impact the transfer length. The 2-D thickness is a major factor impacting overall device performance [6], [63]. One experimental study found that Ti-6L MoS_2 have a larger L_T than that of Ti-2L MoS_2 with the same back-gate overdrive voltage [64]. However, in the top-gate geometries, how a different number of 2-D layers affect transfer length remains unclear. A theoretical study estimated that for monolayer and bilayer 2-D devices with back-gate control, L_T is close to 1 nm, as most carriers would accumulate at the metal-2-D edge (path 1) [61]. However, another experimental study of contact scaling estimated the L_T to be ~35 nm for devices with 2–3 layers MoS_2 in a back-gated geometry [7]. These discrepancies represent the need for further theoretical and experimental investigation of the impact of contact gating and 2-D nanomaterial thickness on the transfer length and carrier injection.

C. Contact Scaling

The advantage of 2-D crystals as a channel material is most obvious in sub-10-nm dimensions as its ultrathinness allows for extremely scaled channel lengths ($L_{ch} \leq 10$ nm), at which silicon (Si) would not be able to achieve satisfactory performance [5], [65], [66]. For a fully scaled device technology, both the channel and contact lengths must be scaled to sub-10 nm. Yet, contact scaling has been largely neglected for 2-D FETs. Papers reporting the most promising performance for 2-D FETs, even at small channel lengths, have contact lengths of hundreds of nanometers to several micrometers [7], [30]. Contact scaling based on the top metal contacts [Fig. 5(a)] has shown severely degraded performance, especially when the contact length L_c (length over which the metal covers the 2-D crystals in the direction of carrier transport) drops below the transfer length, L_T [~30–40 nm for the top-contacted MoS_2 of exfoliated 2–3 layers) [7], as shown in the inset of Fig. 5(b)].

Edge contacts (effective $L_c = 1$ nm) have the potential to yield ultimate scalability, down to sub-5 nm, since the carrier injection area is independent of L_c. Recently, edge contacts to chemical vapor deposition (CVD)-grown MoS_2 films were reported [67], with the device schematics shown in Fig. 5(c). Two edge-contacted MoS_2 FETs ($L_c = 60$ nm and $L_c = 20$ nm) were fabricated on the same 2-D film. Cross-sectional scanning transmission electron microscope (STEM) imaging shows the abrupt interface of the metal contact and edge of the MoS_2 in Fig. 5(d). These two edge-contacted devices, with the same L_{ch} but different L_c, exhibited the same current [Fig. 5(e)] and contact resistance [67]. The fact that device performance can be independent of the physical L_c using edge contacts is encouraging, and further experimental

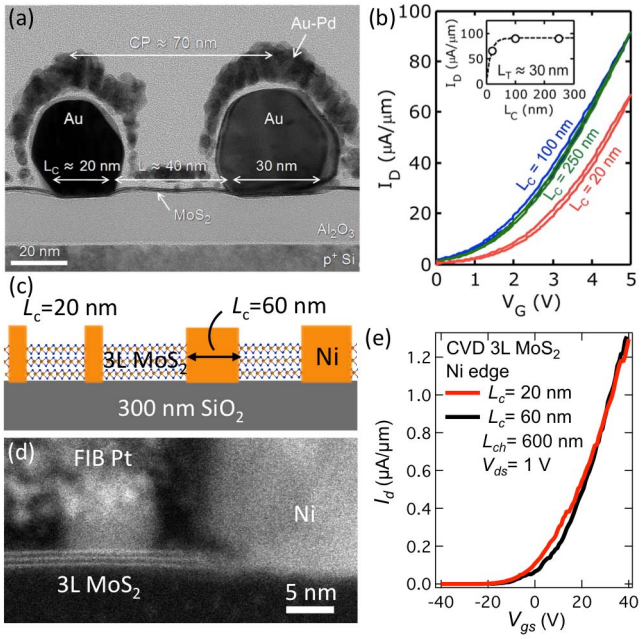

Fig. 5. Scaling contact length in MoS_2 FETs. (a) Cross-sectional TEM image of scaled top contacts. (b) Performance degrades as the contact length decreases. (a) and (b) Adapted from [7] with permission. Copyright 2016 American Chemical Society. (c) Schematic showing edge contacts with different L_C. (d) Cross-sectional STEM images of an edge contact. (e) Similar device performance despite different L_C demonstrates the better scalability of edge contacts. (c) to (e) Adapted from [67].

TABLE I
BENCHMARKING REPRESENTATIVE 2-D FETS

Contact approach	n $\times 10^{12}$ cm^{-2}	I_{on} μA/μm	L_{ch} μm	T_{ch} nm	μ_{FE} cm^{2}V^{-1} s^{-1}	R_c kΩ•μm
[24] Ni etched graphene	4.9	180	0.5	16	80	0.2
[41] 1T MoS_2	6.4	60	0.7	1.4	50	0.2
[30] Cl doping	21.6	410	0.1	4	~55	0.5
[7] UHV Au	9.6	200	0.1	4.5	35	0.74
[68] Ti	12.5	30	1.5	10	~47	0.78
[69] **F4-TCNQ doping+Ni**	**18.0**	**310**	**1.5**	**8.4**	**229**	**0.18**
[70] **Pt/Ni/Al***	**18.0**	**500**	**0.2**	**8**	**50~60**	**0.58**
[71] Ag/Au	18.0	19	4.3	0.7	20~45	~3
[62] Ti/Au	9.5	9	1	0.7	~13	10

For MoS_2 FETs, all I_{on} are extracted at V_{ds} = 1 V. Top metal contacts are used in the reports listed above except in [42], which uses in-plane 1T MoS_2 as the contact.

For BP FETs (bold), all I_{on} are extracted at V_{ds} = -1 V. All the devices listed use top contacts.

The shaded rows represent devices built on CVD-grown MoS_2 films.

*Top gate structure was used, whereas others use back-gate structure.

and theoretical studies investigating the edge interface and improving its performance are needed.

D. From Contact to Device

Instead of benchmarking every available contact approach based only on one or two isolated metrics (typically contact resistance), which has been done to some degree in [14] and [13]. In Table I, we list the state-of-the-art contact engineering progress with emphasis on several key metrics. A selection of the best representative contact engineered MoS_2 and BP FETs was chosen, as these two materials are the most researched 2-D semiconductors and their advances could provide guidelines for other 2-D FETs. Most of the devices listed have contact resistance (R_c) below 1 kΩ · μm, except devices based on CVD films, which are listed in the shaded rows. We include parameters such as channel length (L_{ch}), flake thickness in the channel (T_{ch}), and carrier density (n), where $n = V_{ov}C_{ox}/q$, with overdrive voltage $V_{ov} = V_{gs} - V_{th}$, C_{ox} as the capacitance of the gate dielectric, and q as the elementary charge.

The need for considering the collection of metrics in Table I when analyzing the performance of a given 2-D FET is based on the frequent incongruence of actual device performance (e.g., I_{on}) and favorable metrics (e.g., R_c). For example, phase engineered 1T MoS_2 contacts were reported to yield the smallest contact resistance of 200 Ω · μm, yet produced disproportionately low ON-current, even with a relatively short L_{ch} of 0.7 μm. Cl doping yielded the highestI_{on}, yet it required the highest n of 21.6×10^{12} cm^{-2}. The larger carrier density gives rise to a smaller estimated R_c. As shown in the shaded rows in Table I, devices built on CVD-grown MoS_2 films typically have a higher R_c and more effort is needed to improve the quality of CVD films and subsequent contact interfaces.

Most BP devices show decent ON-current but with small ON–OFF current ratios (on the order of 10^3), even though oxides with equivalent oxide thickness (EOT) of 1–4 nm were used in [70], [72], and [73]. Record low R_c of 180 Ω · μm has been reported, but the F4-TCNQ doping used to realize it also decreases the ON–OFF ratio to 10^2, making this approach less appealing. Extracting I_{on} and R_c before compensating for V_{th} shift and considering the V_{ov} is a common mistake that leads to overestimation in performance related to the contacts [32], [33], [74], [75]. Further exploration is needed to improve the I_{on} for MoS_2 FETs and decrease the I_{off} for BP FETs as they are still far from the target performance outlined in Fig. 2(c) and many simulation studies [76], [77].

Moving forward, when assessing future advances in contact engineering, a comprehensive view must be taken to evaluate the true potential of reported approaches. R_c should be reported together with its associated carrier density, especially in scenarios with contact gating. The impact of device dimensions and contact gating must be accounted for [60] and [61]. Other critical issues, such as variability and yield, may seem less exciting to study, but constitute the most substantial roadblocks for making 2-D electronics a viable technology.

III. GATING OF 2-D FETS WITH ALD DIELECTRICS

Nanomaterials require a protective layer for most applications, whether for passivation, as with BP that degrades rapidly in ambient conditions, or as part of a device, as for all types of FETs [4], [72], [78]–[84]. For most applications, the passivation layer must be dielectric, thin, and high quality; the common approach for obtaining such films is using ALD. While there are other dielectric deposition

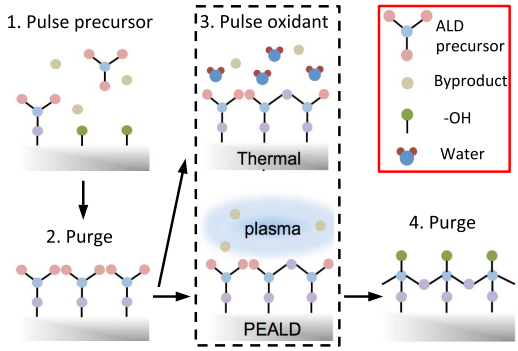

Fig. 6. Basic ALD process flow for a metal oxide showing the two most prominent oxidants that are used: H_2O (thermal ALD) and plasma (PEALD).

approaches under consideration for their use in the 2-D FETs, including transferred 2-D hexagonal boron nitride [85] and the focus herein is on applying the industry-standard approach of ALD for growing high quality, scalable films on the 2-D semiconductors. ALD consists of two-half reactions [86], [87], as outlined for a typical metal oxide growth in Fig. 6. The ALD process results in one uniform layer of film and can be repeated until the desired film thickness is achieved.

The 2-D crystals have a chemically inert basal plane, which presents a significant challenge for nucleating ALD growth. Instead of the precursors reacting uniformly with the surface, they either react with defect sites or are physically adsorbed onto the basal plane [88]–[90]. As a result, ALD does not produce uniform thin films but requires thicknesses >15 nm to realize closed, pinhole-free films [4], [82], [91]–[96]. In order to be able to grow thinner, more scalable, high-k dielectrics, the basal plane must be modified so that the initial ALD precursors are able to react uniformly with the 2-D crystal. Multiple methods have been investigated such as adding a buffer layer, a surface treatment, or changing the oxidants used in ALD. For 2-D FETs, it is important to achieve both a high quality, ultrathin high-k dielectric for the gate stack as well as favorable interfacial properties between the dielectric and 2-D channel (e.g., low-interface trap density). There is little doubt that ALD processes will be critical for any future 2-D-based device, including more unique designs such as the 2-D negative capacitance FETs that rely heavily on ALD films [97], [98] considering the recent success with ultrathin, doped HfO_2 films yielding scalable ferroelectric behavior [99], [100].

A. Surface Treatments

Surface treatments offer one path for enabling growth of thin high-k dielectrics on 2-D crystals by generating more nucleation sites [101]–[111]. The two most prevalent methods of inducing more reactive sites are to expose the surface to ozone under ultraviolet radiation (UV–O_3) or to a plasma [102]–[111]. Surface treatments promote the growth of ALD high-k dielectrics by either creating more defects or by adding adsorbents to the basal plane, which act as reactive sites. Both of these methods have been shown to enhance nucleation on 2-D crystals and enable the growth of thinner,

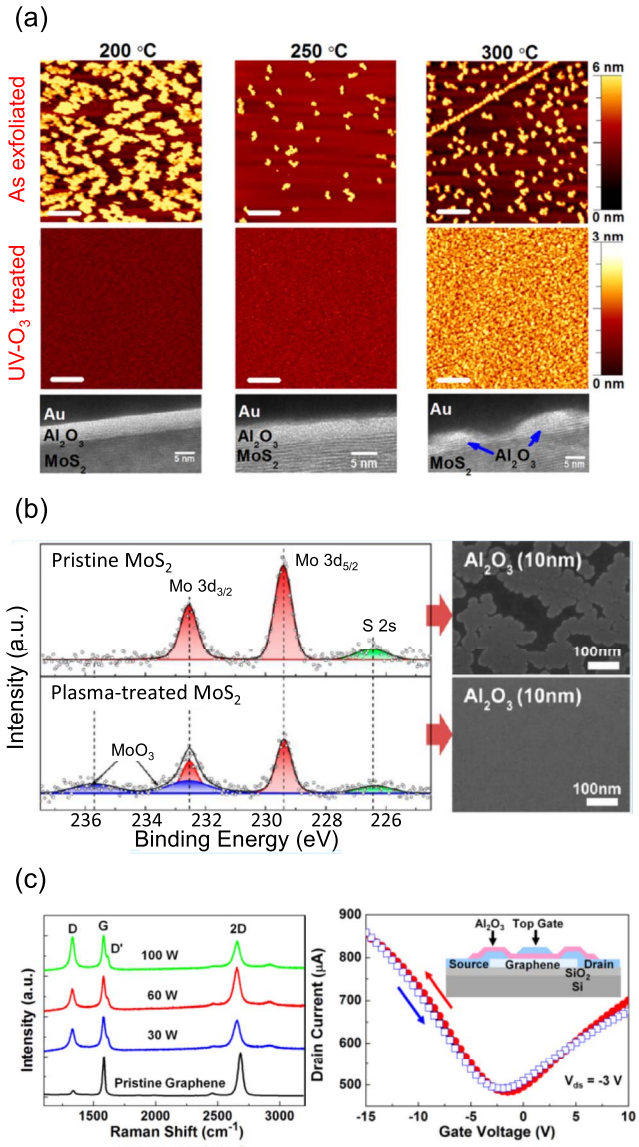

Fig. 7. Surface treatments on 2-D crystals for creating more ALD nucleation sites. (a) AFM and cross-sectional STEM images comparing sample surfaces with and without UV-O_3 treatment before/after the ALD process. Adapted from [109] with the permission of AIP publishing. (b) XPS of MoS_2 with and without the O_2 plasma treatment and evidence of the resultant formation of MoO_3. Adapted with permission from [103]. Copyright 2013 American Chemical Society. (c) Raman spectra of graphene exposed to a N_2 plasma at 30, 60, and 100 W. Top-gate graphene FET characteristics with a gate dielectric of 28 nm deposited after a 100-W N_2 plasma. Adapted from [110] with the permission of AIP publishing.

more uniform high-k dielectrics; however, they both have significant drawbacks.

The use of UV-O_3 treatment has shown potential for MoS_2 [104]–[107], [109], [112], [113], with some reports suggesting that oxygen covalently bonds to the sulfur without the sulfur breaking its bonds to Mo. This would be ideal because the oxygen layer is acting as a sacrificial nucleation layer and, therefore, the underlying MoS_2 is not being damaged. Atomic force microscopy (AFM) and cross-sectional STEM images indicate that 30 cycles of trimethyl aluminum (TMA)/H_2O using a pretreatment of UV-O_3 yields a uniform, pinhole-free dielectric at 200 °C on MoS_2 [Fig. 7(a)]. This functionalization method was used to deposit HfO_2 onto

MoS_2 and fabricate top-gate FETs [33], which had a 10-nm HfO_2 layer, though a 6-nm HfO_2 was said to be obtained. The UV-O_3 treatment process is not consistent and has been shown to form MoO_3 in some reports and oxidize other TMDs such WSe_2 and $MoSe_2$ [104], [106]–[108]. With UV-O_3, the thinnest useable HfO_2 gate dielectric reported is 10 nm, likely owing to unacceptable leakage currents when scaled to 6 nm [50], [105].

Another common type of surface treatment is using O_2 plasma [103], [114]–[116], which greatly improves the nucleation of ALD precursors on the 2-D crystals; however, this is due to the oxidation of the crystal [103], [114]–[116]. O_2 plasmas easily oxidize 2-D crystals, forming oxides such as graphene-oxide on graphene and MoO_3 on MoS_2 [103], [114]–[116]. Obviously, the formation of an oxide layer provides ideal nucleation for growing thin high-k dielectrics. For MoS_2 surface treated with O_2 plasma, smooth 10-nm ALD Al_2O_3 films can be achieved [Fig. 7(b)]. XPS confirms the oxidation of MoS_2 in this process [Fig. 7(b)], making the use of an O_2 plasma pretreatment impractical for growing high-k dielectrics in 2-D FETs, as such damage to the underlying crystal structure, and additional oxide layer in the gate stack, are unacceptable.

Other common plasma treatments include N_2 and H_2 [110], [111], [117], [118]. A N_2 plasma treatment has been shown to provide more nucleation sites for graphene and allow a uniform 28-nm ALD Al_2O_3 film to be deposited [110]. Raman spectroscopy indicates the N_2 plasma creates defects as a more pronounced D peak is observed with increased plasma power; however, the weakness of the D peak indicates that a reasonable amount of the graphene retains its crystallinity [Fig. 7(c)]. The effect of N_2 plasma has also been examined on MoS_2 [117], where it was found that 50 W of N_2 plasma for 5 min increased the rms of MoS_2 from 1.1 to 1.5 nm, indicating considerable damage to the crystal. A H_2 plasma pretreatment on graphene has also been used prior to the deposition of 8-nm ALD Al_2O_3 [111]. Raman showed that the hydrogenation of graphene was reversible after the ALD Al_2O_3 and annealing at 400 °C; however, no devices were made to test the robustness of the gate dielectric. While this process may work for graphene, it does not translate to other 2-D materials such as WSe_2. One report found that just 1-min H_2 plasma exposure on WSe_2 in an FET severely degrades its back-gate and top-gate electrical properties [118]. While the use of surface treatments aid in the process of growing more scalable ALD high-k dielectric films, they come at the cost of damaging the underlying 2-D crystal.

B. Buffer Layers

In order to provide more nucleation sites, a buffer layer can be deposited or grown onto the 2-D crystal prior to ALD. This functionalization method is straightforward, easy to implement, and typically causes little damage to the underlying 2-D crystal. Buffer layers must be insulating, able to be deposited in thin films, and provide enough nucleation sites such that the ALD precursors react with the surface more uniformly. Common buffer layers include metal oxide layers [17], [39]–[43] and organic layers [90], [119]–[123]. A notable shortcoming

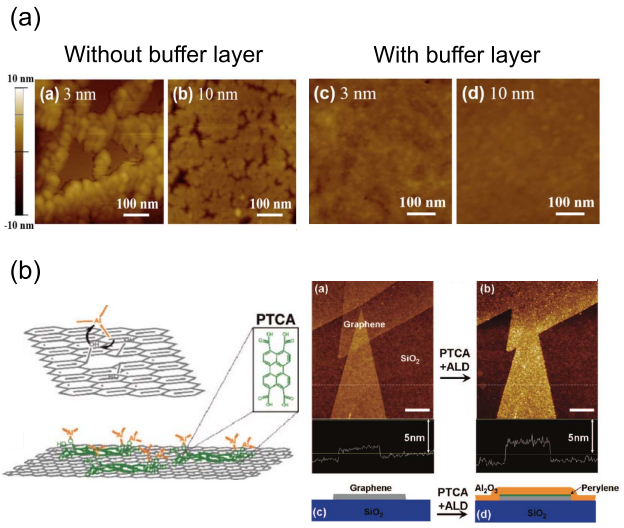

Fig. 8. Buffer layers for nucleating ALD growth. (a) AFM image showing comparison of MoS_2 with and without a metal oxide buffer layer prior to the deposition of 10-nm ALD Al_2O_3. Adapted from [124] with the permission of AIP publishing. (b) Due to the nature of PTCA, the molecules lie flat on the graphene surface with functional groups that react more readily with ALD precursors out of plane. Adapted with permission from [90]. Copyright 2008 American Chemical Society.

to using buffer layers for ALD nucleation is that they add to the overall gate-stack thickness and thus increase the EOT for a 2-D FET, compromising the electrostatic gate control to some degree.

For metal oxide buffer layers, a metal seeding layer (1–3 nm) is formed and allowed to naturally oxidize prior to ALD [80], [124]–[134]. Typically, the metal corresponds to the metal oxide to be deposited. Once the metal is naturally oxidized, there are a plethora of nucleation sites for the ALD precursors, resulting in thinner, uniform ALD films [124]. AFM images in Fig. 8(a) show how the addition of a metal buffer layer yields more uniform ALD films on the top of the oxidized seeding layer, down to 3 nm [124]. Due to the nature of the buffer layer, higher ALD temperatures can be employed since there is no chance of the metal-oxide-seeding layer being desorbed as with organic buffer layers [90], [119], [121], [122], [124], [135]. The use of higher ALD temperatures typically results in a higher quality dielectric [86], [124], [136]. Al, Ti, and Ta seeding layers on graphene have been studied [125] and while Raman showed Al and Ti to have little impact on the crystal structure, cross-sectional TEM shows the top graphene layer has more defects than the underlying layer, and that Ta caused the most damage. Similar to a metal oxide, graphene oxide has also been used as a buffer layer [114], where a bilayer graphene stack was exposed to an O_2 plasma, such that only the top layer was converted into graphene oxide [114]. Overall, while the use of metal oxide buffer layers creates more nucleation sites and allows for more uniform ALD, when the metal seed layer oxidizes it expands, inducing strain and lattice disruptions that can alter the 2-D crystal's electrical properties [137]–[139].

Another type of buffer layer is organic films, such as those formed by exposing the 2-D crystal to an acid like 3, 4, 9, 10-perylenetetracarboxylic acid (PTCA) or polymer mixture

[90], [119], [121], [122], [135] prior to ALD. In the case of treating graphene with PTCA or perylenetetracarboxylic dianhydride (PTCDA), the molecules noncovalently bind with the graphene surface and have functional groups that easily and uniformly react with the precursors to yield thin ALD films (∼3 nm) and low rms, though no top-gate FETs were fabricated to test the robustness of the dielectric [Fig. 8(b)] [90]. Johns *et al.* [121] found that the PTCDA is not consumed during the ALD process; rather, the water precursor is physically adsorbed onto the PTCDA molecules. Other organic layers include polymers that can be spun on like photoresist [120], [140], [141]. Photoresist has been used to not only pattern graphene, but also to act as a nucleation layer for ALD [140], [141]. These polymeric buffer layers tend to be thick (>10 nm) and are, therefore, not particularly useful for scaled dielectrics on 2-D crystals. Polymer-based buffer layers also have a much lower dielectric constant than typical high-k dielectrics, resulting in a much higher EOT of the gate stack. The use of organic buffer layers also requires a low ALD temperature so that the molecules do not desorb, which is not ideal since dielectric films deposited at lower temperatures tend to have a higher density of defects.

C. Modifying the ALD Process

Another way to produce scalable ALD dielectrics is by modifying the ALD process itself by changing the oxidant, which in thermal ALD is typically H_2O vapor [Fig. 9(a)]. One alternate oxidant is ozone (O_3), which has enabled thinner ALD films on graphene and MoS_2 [142]–[144]. For both graphene and MoS_2, the first few cycles are done at a low temperature to ensure the O_3 does not react or desorb. After these first few cycles, a higher deposition temperature may be used to improve dielectric quality [142]. Using O_3 as the oxidant, a ∼4.5-nm (∼5.1 nm) Al_2O_3 film has been deposited onto graphene (MoS_2) [142]–[144]. AFM images confirm that using O_3 as an oxidant compared to H_2O results in smoother films [Fig. 9(a)] [143]. The XPS O 1s peak shows a greater number of intermediate species (peak at 533.1 eV) occur in the O_3 films versus H_2O due to incomplete reactions between the metal organic precursor and the oxidant.

A second alternative oxidant source is plasma called plasma-enhanced ALD (PEALD) and has been used to deposit high-k dielectrics on graphene and MoS_2 [145]–[147]. Generally, PEALD has many advantages over thermal ALD, such as lower deposition temperature, higher variety of films, fewer contaminants, and faster deposition rate [87]. The plasma used is remote; however, plasma damage is still a concern. For the case of graphene, Raman revealed intact monolayer graphene following a PEALD process; however, there was an increase in the D peak indicating an increase in disorder [145]. Fig. 9(b) shows the AFM images of 10 nm of ALD versus PEALD Al_2O_3 on graphene. Fig. 9 shows the transfer curves comparing PEALD Al_2O_3 to e-beam evaporated SiO_2.

In the case of MoS_2, a sub-5-nm gate dielectric has been deposited using PEALD. This scaled dielectric proved to be robust and pinhole free, as it was used as a gate dielectric in a top-gated MoS_2 FET [Fig. 9(c)] [147]. The actual gate dielectric thickness was found to be ∼3–4 nm, as confirmed

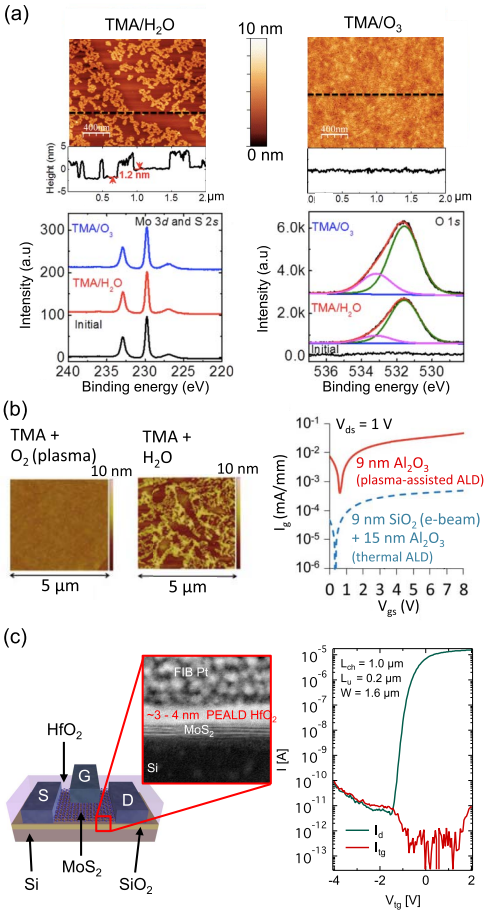

Fig. 9. Nontraditional oxidants used in ALD on 2-D crystals. (a) AFM images of MoS_2 with 30 cycles of ALD using TMA/H_2O compared to MoS_2 with five cycles of ALD using TMA/O_3 at 30 °C followed by 45 cycles of ALD at 200 °C. Replacing the H_2O oxidant with O_3 yields uniform films of ∼5 nm. XPS spectra indicate MoO_3 is not formed while Al-O is formed; however, the higher binding energy peaks indicate a higher concentration of incomplete reactions between TMA and O_3 compared to TMA and H_2O. Adapted with permission from [143]. Copyright 2014 American Chemical Society. (b) AFM images show the stark contrast between using O_2 plasma versus H_2O as oxidants to grow 10-nm ALD Al_2O_3 on graphene. I_d–V_{gs} curves indicate the difference between using 9 nm of PEALD Al_2O_3 and 9-nm e-beam SiO_2 capping layers. Adapted with permission from [145]. Copyright 2011 IEEE. (c) Top-gate MoS_2 FET schematic with a close up of the interface between the MoS_2 and PEALD HfO_2 clearly showing the dielectric layer is between 3 and 4 nm thick. Top-gate electrical characteristics show strong gate control and low leakage current. Adapted with permission from [147]. Copyright 2017 American Chemical Society.

by the cross-sectional STEM. The PEALD HfO_2 process even improved the back-gated electrical properties of the MoS_2, through the potential for some damage to the 2-D crystal remains uncertain [147]. Most studies have been performed on multilayer films, whereas monolayer would provide more definitive evidence of any plasma damage. One way to mitigate possible plasma damage is to use a metal seeding layer prior to PEALD [118]. Further exploration is needed of PEALD processes for growing ultrathin, high-k dielectrics on 2-D crystals.

IV. Prospect

Significant advancements have been made to engineer better contact and gate interfaces to 2-D nanomaterials. Research

groups have been able to demonstrate low contact resistance and reasonably high ON-current, but rarely simultaneously; and even when considered independently, both of these metrics are still far from the desired values. Moreover, there needs to be consideration of the variability and yield for the proposed improvements to the metal-2-D contact, along with a more comprehensive theoretical picture of transport at this unique interface to account for parameters such as gating configuration and the number of 2-D layers. Recent data suggests that pure edge contacts offer ultimate scalability for 2-D FETs and warrant further pursuit. Gating of 2-D crystals has also come a long way, with advancements in the ALD growth of ultrathin, high-quality dielectrics on the inert 2-D surfaces. While PEALD processes show the most promise for ultimately scaled films, there remains much to be learned about the interface between the 2-D crystals and PEALD dielectrics. In regards to both contacting and gating 2-D nanomaterials, there is no doubt the unique features of the 2-D basal plane will continue to be a source of frustration while also presenting a potential opportunity for discovering novel solutions for future devices.

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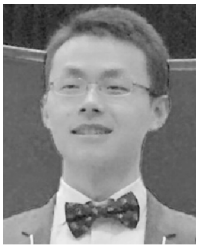

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