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Immunity to Contact Scaling in MoS_2 Transistors Using in Situ Edge Contacts

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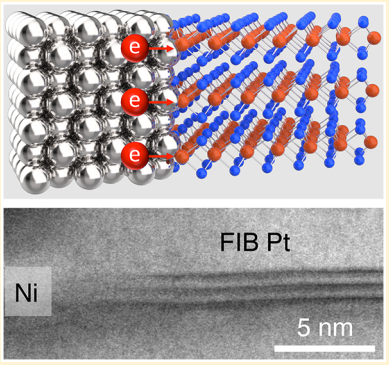
Supporting Information

ABSTRACT: Atomically thin two-dimensional (2D) materials are promising candidates for sub-10 nm transistor channels due to their ultrathin body thickness, which results in strong electrostatic gate control. Properly scaling a transistor technology requires reducing both the channel length (distance from source to drain) and the contact length (distance that source and drain interface with semiconducting channel). Contact length scaling remains an unresolved epidemic for transistor scaling, affecting devices from all semiconductors—silicon to 2D materials. Here, we show that clean edge contacts to 2D MoS_2 can provide immunity to the contact-scaling problem, with performance that is independent of contact length down to the 20 nm regime. Using a directional ion beam, in situ edge contacts of various metal−MoS_2 interfaces are studied. Characterization of the intricate edge interface using cross-sectional electron microscopy reveals distinct morphological effects on the MoS_2 depending on its thickness—from monolayer to few-layer films. The in situ edge contacts also exhibit an order of magnitude higher performance compared to the best-reported ex situ metal edge contacts. Our work provides experimental evidence for a solution to contact scaling in transistors, using 2D materials with clean edge contact interfaces, opening a new way of designing devices with 2D materials.



KEYWORDS: *2D materials, in situ edge contacts, contact scaling, splitting 2D crystals, metal−2D interfaces*

Booming applications, such as smartphones, autonomous vehicles, and server farms, leave society starving for more computational power. At the heart of virtually all computation is the transistor, which yields increased computational ability with each successive technology node through size scaling. Such scaling, which enjoyed decades of success predicted by Moore's law, is now undisputedly slowing and potentially reaching an end based on the limitations of silicon.[1−5] Not surprisingly, the electronic device community has been eager to explore new materials for the transistor channel that may extend the scalability roadmap, even for a few more generations. Nanomaterials have long been seen as a viable option, from 1D carbon nanotubes to the expanding family of 2D crystals. For 2D, graphene initially captured widespread attention and spawned a whole library of 2D materials with a variety of electronic band structures and properties.[6−11]

The main advantage of 2D materials is their ultrathin nature, which could enable extremely scaled transistors for the "Beyond Moore" era. The ultrathin body thickness directly affects the screening length, which dictates how short the channel length can be scaled down without inducing deleterious short channel effects. Using a planar device structure, it is estimated that monolayer MoS_2 has a screening length of less than 1 nm,[12] assuming an equivalent oxide thickness (EOT) of 1 nm is used. This suggests that the gate-tunable, 2D-based transistor can be scaled to sub-5 nm channel length—a scale where Si encounters severe short channel effects using similar gate structures. Both experimental and theoretical studies have demonstrated the superb channel length scalability of 2D field-effect transistors (FETs).[12−18] Aside from the superior scalability, 2D materials also offer new possibilities for other unconventional applications (for example, flexible electronics) because of their substrate independence.[19−21] Moreover, a plethora of atomic heterostructures can be formed between different 2D materials,[22−26] in a way that is inaccessible to traditional semiconductors.

While the scalability of channel length in 2D FETs has been well studied,[13−15,17,18,27] the contact length and its related scaling challenges have been largely neglected. However, contact engineering in general for 2D FETs has been a topic of discussion,[28−31] as well as using different metals,[32,33] transforming phases,[34] and interface engineering.[11,35] While these approaches deepen our understanding of the metal−2D interface and have achieved contact resistance as low as 200

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Ω·μm, they all use a contact length of at least hundreds of nanometers, which is orders of magnitude larger than needed for actual technologies. A fully scaled device technology for the 2030 era will require both the channel and contact lengths to scale below 12 nm (equivalent to a contacted gate pitch of 24 nm).[36] Note that contact scaling is also a pressing challenge for traditional Si technology. In a Si FinFET, the contact length (36 nm) occupies two-thirds of the gate pitch (54 nm for Intel's 10 nm node technology).[37] Since future scaled transistors (including traditional Si-based devices) would have a shorter gate pitch, the shrinking gate pitch also leads to shrinking contact length, thus decreasing on-state performance[38] and highlighting the importance of contact scaling. In a simplified top-contacted and back-gated MoS_2 transistor, as shown in Figure 1a, as the contact length (L_c) decreases, the

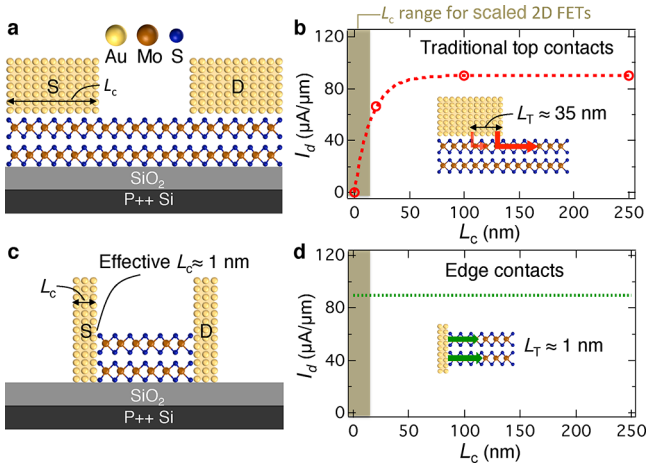

Figure 1. Top versus edge contacts to 2D MoS_2. (a) Schematic of a bilayer 2D FET with traditional top contacts. (b) On-current diminishes as the top contact length decreases (data from ref 35), presenting a major roadblock for aggressively scaled transistors. Transfer length is indicated in inset schematic. (c) Schematic of a bilayer 2D FET with edge contacts and an effective $L_c \approx 1$ nm, leading to the possibility of (d) on-current that is independent of contact length. The on-current values in panel (d) are hypothetical.

area available for carrier injection is also reduced. The shrinking contact length leads to severely degraded performance, especially when L_c drops below the transfer length (L_T = 30–40 nm for MoS_2,[35] as depicted in Figure 1b), which is the length over which the majority of carriers are injected.

Ideally, for scaling, contacts would be bonded directly to the side of the 2D channel as pure "edge contacts," as illustrated in Figure 1c, where charge is injected from the metal directly into the 2D crystal via covalent bonds. Since the area of injection at the edge is independent of the physical contact length, we hypothesize that edge contacts could provide ultimate scalability, as shown hypothetically in Figure 1d, where the on-current (I_d) would be independent of the L_c. Several studies on edge contacts to 2D materials have been reported, beginning with Cr edge contacts to graphene that exhibited a low contact resistance of 150 Ω·μm,[39] though graphene is not a semiconductor. A decade before MoS_2 was considered as a transistor channel material, MoS_2 edges were explored, with results indicating that one-dimensional metallic states can be identified due to the band structure changes significantly at the edge.[40] In a separate study,[41] an edge-like contact interface between graphene and MoS_2 was demonstrated; however, the MoS_2–graphene junction spans ~20 nm and the scalability of this approach is uncertain. Moreover, growing the graphene–MoS_2 edge added additional complexity and variability to the fabrication process, reducing the reliability of this approach. Hybrid top and edge contacts have been proposed,[42,43] but the current crowding effect caused by the application of V_{ds} at the contact promotes carrier injection through the top contact interface instead of the edge interface, casting doubt on whether the edge contact interfaces are providing any real benefit. Finally, demonstration of edge contacts between metal and MoS_2 has been limited to the use of an *ex situ* and isotropic plasma etching approach.[44] The performance metrics such as on-current and on–off ratio were unfavorable, possibly due to the uncleanliness of the interface with the dangling bonds in the exposed MoS_2 edge reacting with species in the ambient owing to the use of an *ex situ* plasma etching. Considering the ultrasensitive nature of the dangling bonds at the edge, it is thus crucial to have the interface preserved in a clean *in situ* environment in order to properly determine the potential of metal–MoS_2 edge contacts.

Here, we demonstrate edge-contacted MoS_2 FETs by using an *in situ* Ar ion beam. We show the ultimate scalability of pure edge contacts to CVD-grown MoS_2 of various layer thicknesses and metal types, providing evidence for the immunity of edge-contacted 2D FETs to aggressive contact scaling. In order to understand carrier transport at the edge interface, we use cross-sectional scanning transmission electron microscopy (STEM) and low-temperature electrical measurement to characterize the edge contacts. Our study elucidates the intriguing metal–2D edge interface and the potential of edge contacts for future scaled transistors.

Etching Capability of a Directional Ar Ion Beam. The use of an *in situ* ion beam to etch the MoS_2 immediately prior to contact metallization is crucial to avoid reactivity between the created edge states and molecular species other than the contact metal. The *in situ* ion beam source is incorporated with an electron beam evaporator in the same ultrahigh vacuum (UHV) chamber, as shown in Figure 2a. The etching effect of the ion beam on MoS_2 is studied using the process shown in Figure 2b. Selective bombardment of the exposed (contact) regions by the directional Ar ion beam is achieved using patterned PMMA (which shields the channel regions). Note that the Ar ion beam has a minimal etching effect on the PMMA, which make PMMA a suitable etch mask, as shown in Figure S6. Our previous study[45] shows that low-energy (~100 eV) Ar ion bombardment can create vacancies in the 2D crystal. Here, a higher energy (~600 eV) ion beam is shown to controllably etch the MoS_2, as shown in the atomic force microscopy (AFM) image in Figure 2c. We also use energy dispersive spectroscopy (EDS) to map the etched flake in Figure 2c. The sulfur signal in Figure 2d and molybdenum signal in Figure 2e further prove the etching capability of the Ar ion beam. The AFM profiles and line scans from different regions show how both the MoS_2 and SiO_2 are etched by the ion bombardment, as plotted in Figure 2f. Note that the edge of MoS_2 in the etched region attracts more reacted species/residue (as high as 100 nm in Figure 2g) compared to the SiO_2 etched edge, evidential of the higher reactivity of the MoS_2 edge when exposed to solvent/air (ex situ) and the importance of forming edge contacts with an in situ process. Meanwhile, the flake edge that has not been exposed to the ion beam is relatively clean, as shown in Figure 2g. This further exemplifies the highly reactive etched edge, which could be useful in other

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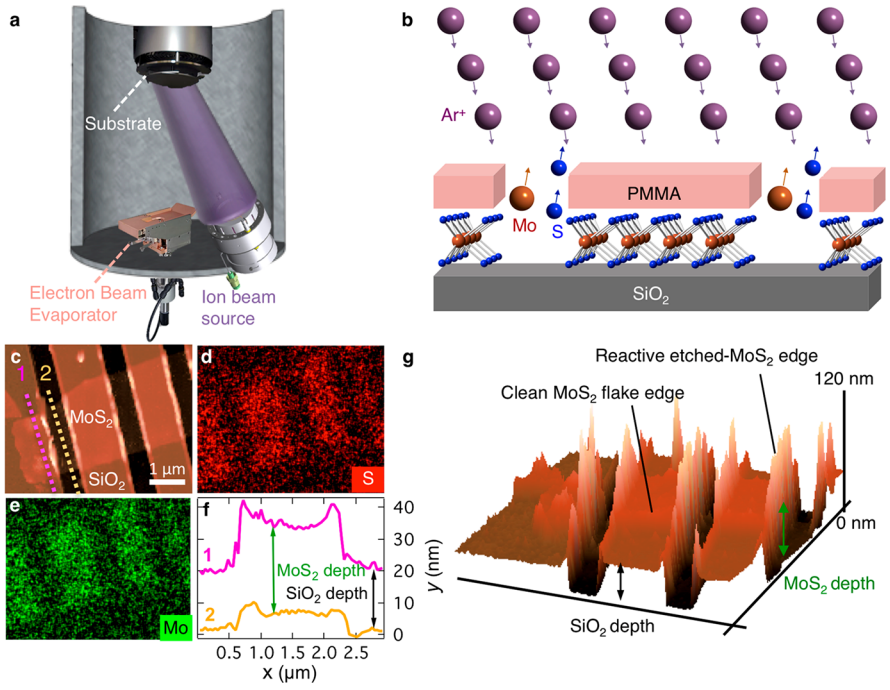

Figure 2. In situ etching of MoS_2. (a) Ion beam source and e-beam evaporator incorporated within the same UHV chamber. (b) Schematic of the etch process with only contact regions selectively bombarded by Ar ion beam. (c) AFM image of MoS_2 flake after etching and PMMA removal. EDS mapping of the flake in panel (c) gives the sulfur signal in panel (d) and molybdenum signal in panel (e). (f) Line scan height profiles 1 and 2 from the AFM image in panel (c). (g) Three-dimensional AFM image of panel (c) highlighting the reactive etched MoS_2 edges and the relatively clean MoS_2 flake edges.

applications such as sensing. The edge sites could act as a preferable binding site for antibodies compared to either the basal surface that has limited dangling bonds or the natural edges that are less reactive. In Figure 2g, we also label the SiO_2 and MoS_2 etched depth shown in Figure 2f. The relationship between the etch-depth and the ion beam exposure time is plotted in Figure S7.

Edge Contacts to Exfoliated Multilayer MoS_2. Upon exposing the MoS_2 edge in the contact regions under UHV, contact metal is then deposited using an electron beam evaporator in the same chamber. The newly generated edge states are able to react with the depositing metal, forming a bonded edge interface. To study this interface, we use cross-sectional scanning tunneling electron microscopy (STEM) to characterize the etched edge. Fifteen layers of MoS_2 were exfoliated onto a silicon wafer with 300 nm SiO_2 (see cross-sectional STEM image in Figure S8). After using the etching process illustrated in the last section, the metal contact was *in situ* deposited on the etched region (Figure 3a). The cross-sectional STEM image of the finished contact is shown in Figure 3b. The etching process creates the unique splitting and tapering effects (Figure 3c), which is particularly surprising as these effects are different from the common undercut[46] and microtrench[47] profile seen in some isotropic ex situ plasma processes. The splitting effect could be attributed to the interaction between the directional Ar ion beam and the weak van der Waals interlayer binding of the 2D materials. The splitting effect could profoundly change electronic properties of the MoS_2 at the edge (further details in Note S1). Meanwhile, the tapering effect is common for directional dry etching,[48] as the center region receives more directional ion bombardment. These effects open a new window of opportunities to study the intricate interface between metal and 2D materials and to use in other applications such as sensing and material intercalation.[49−51]

To further understand the metal−MoS_2 edge interface, EDS was used to characterize the elements present in the right-side edge of the contact. As shown in Figure 3d, the MoS_2 is topped with 2 nm of Ti (green) and 20 nm of Au (red). The thickness of Ti is more uniform in the area where there is more MoS_2 edge in the splitting and tapering region, indicative of more consistent bonding because of the reactive edge states. The combined elemental map shown in Figure 3d may suggest that sulfur is concentrated at the splitting interface, but the individual sulfur map in Figure S9 shows that the distribution of sulfur within the metal region after etching is actually quite even. Also, the oxygen was mapped in Figure S9, and no higher concentration appears in the interface between Ti and MoS_2, which suggests that the *in situ* environment is relatively pristine.

In addition to the interface highlighted in Figure 3, where the full multilayer MoS_2 is etched by the Ar ion beam in the center of the contact regions (quasi-edge contacts), we also used shorter etching time (25 and 50 s) to produce partially etched MoS_2 in the center of the contact region (partial-edge contacts), as given in Figure S10. Since the exfoliated flake is about 10 nm thick (15L), the tapering and splitting effects in Figure 3 also show up in the partial-edge contacts. We then fabricated devices on multilayer flakes with different thickness (35 and 8 nm) in order to compare performance of the quasi-edge and partial-edge contacts (see Notes S1−S2). Compared to the partial-edge contacts (9 μA/μm at V_{ds} = 1 V), quasi-edge contacts yield smaller current (5 μA/μm at V_{ds} = 1 V) but have a distinct forming or "burn-in" effect when large V_{ds} (over 3 V) is applied. This forming behavior suggests that a large electric field from source to drain can strengthen the bond

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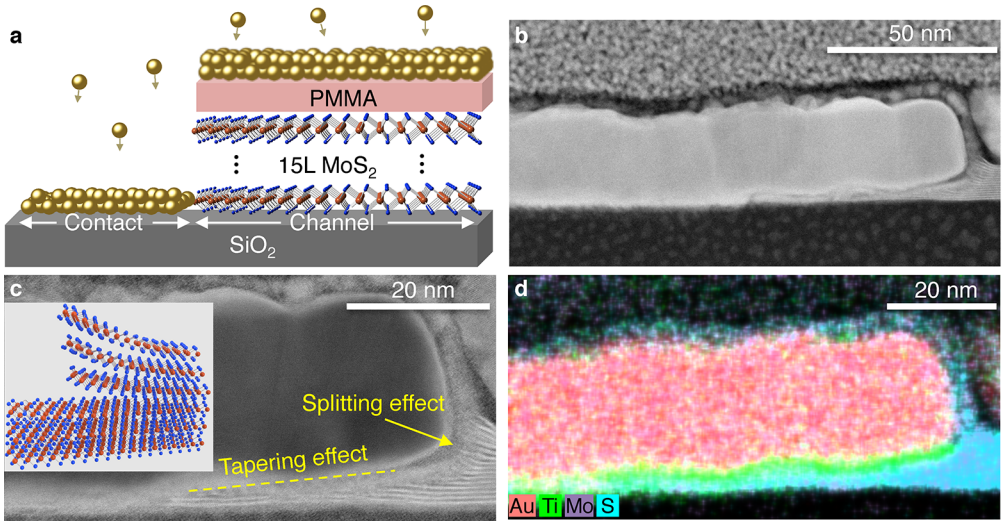

Figure 3. Metal edge interface to multilayer MoS_2 flakes. (a) Diagram of the *in situ* metal deposition process forming an edge contact for 15L MoS_2 flake with 2 nm Ti/20 nm Au. (b) Cross-sectional STEM image of L_c = 200 nm contact. (c) Magnification of left edge of the contact showing tapering and splitting effects. Inset image showing the splitting effect for MoS_2 crystal. (d) EDS image of right side of the contact mapping the presence of different elements.

between the metal and MoS_2 edge states. Considering that the defects created on the tapering region add additional complications to the analysis, further investigation is needed to resolve the carrier injection through the splitting MoS_2 edge and the tapering layers. In the following section, in order to demonstrate pure edge contacts and their scaling behavior, we focus on CVD-grown MoS_2 films since they offer a large area of thin crystals (1−4 layers with size of over 100 μm^2).

Edge Contacts to CVD-Grown MoS_2 (As Grown on SiO_2). In order to demonstrate the ultimate scalability of edge contacts, *in situ* edge contacts were fabricated on CVD-grown MoS_2. These MoS_2 films have a large area with uniform thickness, making them suitable for device fabrication and performance comparison. Trilayer and monolayer CVD films were used to fabricate *in situ* edge contacts as shown in Figure 4. These films were grown directly onto SiO_2 without the need of a transfer process, which could introduce contaminants such as water molecules and resist residue. In Figure 4a, a small rectangular box of MoS_2 was used, as the materials outside of the rectangular box are etched away using CF_4 plasma. After an e-beam lithography process, the same Ar ion beam etching process to Figure 2b with an etching time of 30 s was used and the contact metal (Ni) was deposited *in situ* inside the same UHV chamber. A diagram of scaled edge contacts to MoS_2 is given in Figure 4b, where two long contacts (L_c = 60 nm) and two short contacts (L_c = 20 nm) were fabricated onto the same film. The cross-sectional STEM image of the right-side of the L_c = 60 nm edge contacts is shown in Figure 4c. The metal entrenches into the oxide and contacts the edge of the trilayer film without the splitting effect, producing pure edge contacts. The side-view of the three-layer MoS_2 film with atomic resolution is given in Figure 4d, showing the crystal structure of the 2D material. Characterization of the devices with different contact lengths (Figure 4e,f) revealed that the L_c = 20 nm and L_c = 60 nm FETs have the essentially same I_d, independent of the contact length. One of the most encouraging aspects of this result is the sheer density of carriers being injected into the edge contact area (effective L_c = 1 nm), which is over an order of magnitude smaller than the top contact L_c using the same film and 2 orders of magnitude smaller than the top contact L_c used in other studies.

Edge contacts to monolayer MoS_2 from CVD-grown crystals were also explored. A device structure similar to the one illustrated in Figure 4a was used, with monolayer MoS_2 as the channel material (Figure 4g). A triangular monolayer film was chosen, and the same process of *in situ* etching and metal evaporation was used to make the edge contacts with different contact lengths. The cross-sectional STEM images show the metal entrenching into the oxide, representative of complete MoS_2 removal in the contact region. To avoid damaging the bottom oxide, shorter exposure time can be used. In Figure S12, we used 5 s of 600 eV Ar ion beam and found that 2L MoS_2 can be etched. No significant aspect ratio-dependent etching was observed from our study using directional ion beam etching compared to traditional plasma etching.[52] Additionally, our recent study shows that 3 s of 60 and 200 eV Ar ion beam are capable of etching away 1L MoS_2.[53] Hence, the damage to the bottom SiO_2 should be minimal considering the short exposure time (see Figure S7 for reference). EDS images of the contact (Figure 4i) provide further evidence of the isolation of the MoS_2 to the channel and the abrupt contact interface. A magnified view of the sulfur at the edge is given in Figure S11, further showing this abrupt cutoff of the monolayer MoS_2 at the edge. The corresponding I_d−V_{gs} curves for the monolayer MoS_2 devices are given in Figure 4k−l. The corresponding I_d−V_{gs} curves for the monolayer MoS_2 devices are given in Figure 4k−l. The difference in the off-current in Figure 4k is attributed to device-to-device variation as no clear relationship between off-current and contact length was observed. Possible explanations for the low performance observed in the edge-contacted 1L MoS_2 will be discussed in coming sections.

The effect of different metal types is also important in understanding the in situ edge contact scheme. The I−V characteristics of Au, Cr, and Ni are compared in Figure S13. After shifting V_{th}, Cr yields similar performance compared to Ni. This result is in contrast to the previous study where Cr is shown to outperform the other metals when contacting graphene through the edge,[39] which indicates the edge contact

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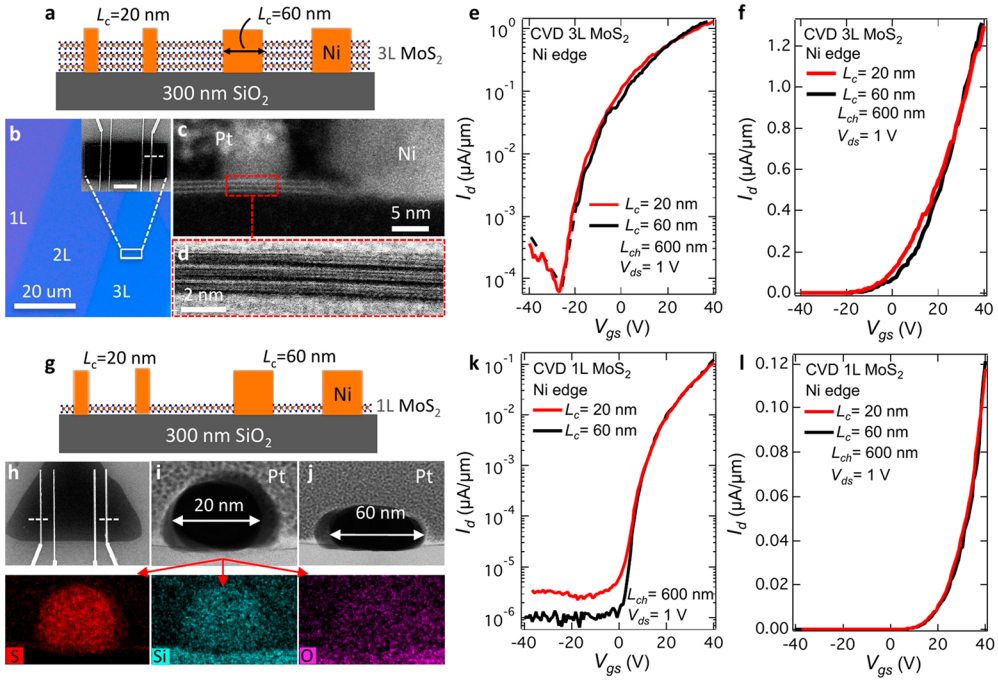

Figure 4. Trilayer and monolayer MoS_2 FETs with Ni edge contacts. (a) Schematic of edge-contacted devices on 3L MoS_2. (b) Optical image of CVD-grown flakes with inset SEM image of trilayer MoS_2 FETs; scale bar in SEM image is 1 μm. Cross-sectional STEM images of (c) right edge of L_c = 60 nm contact and (d) atomic side-view of the trilayer MoS_2. (e) Subthreshold and (f) transfer characteristics of the edge-contacted devices, showing performance that is independent of contact length. (g) Schematic of edge-contacted devices on monolayer MoS_2. (h) SEM image of the devices with a scale bar of 1 μm. STEM images of (i) L_c = 20 nm contact and (j) L_c = 60 nm contact. Arrows point to corresponding EDS scans of sulfur, silicon, and oxygen in panel (i). (k) Subthreshold and (l) transfer characteristics of the monolayer edge-contacted devices, also showing the performance that is independent of contact length.

performance is dependent on the 2D materials properties. Theoretically, Cr has been proposed to be an ideal metal to contact MoS_2 in the top contact scheme, with its shorter bond length to S, larger binding energy, and larger density of state at E_F.[54] As the bonding length could be shorter in the edge contact scheme, density functional theory (DFT) calculations on Cr edge contacts to MoS_2 remain to be conducted in order to confirm the orbital overlapping profile. To further understand the *in situ* edge contact, we characterized Cr edge contacts under low-temperatures. As given in Note S5, a relatively small Schottky barrier height of 11.7 meV is extracted. Note that the exact barrier profile may be different from traditional top contacts due to the different bandgap at the termination of MoS_2 in addition to different carrier injection mechanism. A focused theoretical study is warranted to investigate the impact of edge interfaces on the band structure and carrier transport of metal−2D edge contacts.

The performance of the edge contacts discussed above is lower than that previously reported for top contacts using the same contact metals.[45,55] From the data presented thus far, one might conclude that edge contacts inherently lead to lower performance due to the decreased area for carrier injection at the edge interface compared to a top contact interface. Alternatively, the quality of the CVD as-grown MoS_2 could be relatively poor considering the likely high density of interface traps formed between SiO_2 and MoS_2 during the high-temperature CVD growth process. To investigate which factor plays a major role, we fabricated both top- and edge-contacted devices on the same as-grown 1L MoS_2. The device performance (plotted in Figure S14) shows that the top- and edge-contacted devices demonstrate similar performance, indicating that the quality of the as-grown MoS_2 film could be the major factor limiting the performance of the devices presented above. Hence, in the following section, we use transferred MoS_2 rather than as-grown MoS_2 for the channel material.

Scaling Edge Contacts to CVD-Grown MoS_2 (Transferred onto SiO_2). Devices fabricated on as-grown MoS_2 suffer from low performance and high variability.[56] As mentioned previously, the reason behind the inferior devices could be the higher density of interface traps between the MoS_2 and the SiO_2 substrate. These interface traps can be induced by the high-temperature CVD process.[56] To address this issue, we transferred SiO_2-grown MoS_2 onto a fresh SiO_2 surface using a water-assisted transfer technique.[57] Ni top-contacted devices were fabricated both on the as-grown MoS_2 and the transferred MoS_2 for comparison. Devices with transferred MoS_2 yield higher performance and smaller variability (Figure S15), consistent with ref 56.

The contact length for edge contacts was varied to determine the scalability of the edge contact scheme. On a transferred CVD-grown 1L MoS_2 film, *in situ* Ni edge contacts were fabricated with different contact lengths, while the channel length remained constant (Figure 5a). The I_d−V_{gs} curves of the Ni edge contacts with different L_c are plotted in Figure 5b. The devices with different L_c have a similar I_d−V_{gs} profile, indicative of the true edge profile and pure edge injection of carriers since there is invariance with contact length change, as plotted in Figure 5d. Of note is that the performance achieved is 70 times higher than the device built on as-grown MoS_2. The I_d−V_{ds} curves in Figure S16 show a slight nonlinearity in the low V_{ds} regime, suggesting a slight barrier for carrier injection in the edge contact interface. To further confirm the scalability of edge contacts, we fabricated

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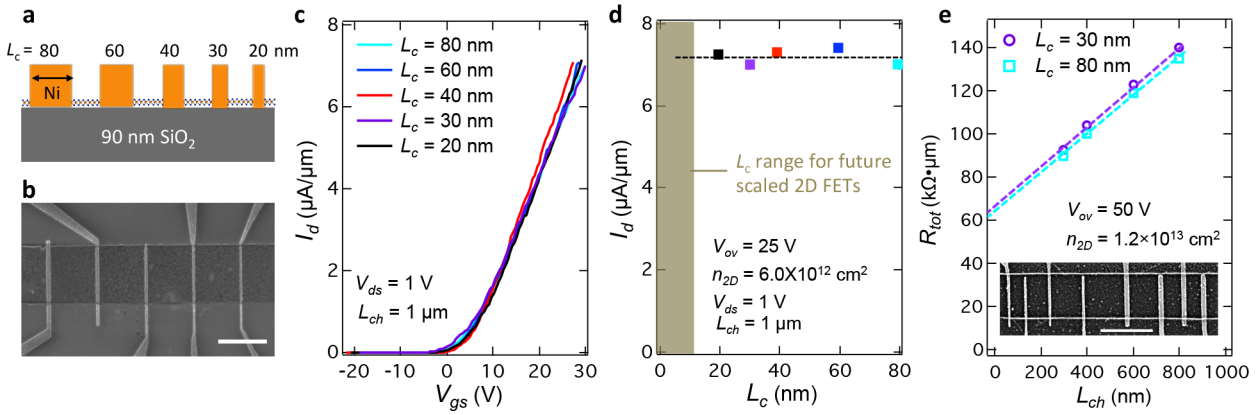

Figure 5. Scaling of contact length for in situ edge contacts. (a), Device schematics of the scaled Ni edge contacts to 1L MoS_2 FETs. (b) SEM image of the devices in panel (a). Scale bar, 1 μm. (c) Example transfer curves of edge-contacted devices. (d) Relationship between I_d and L_c for in situ edge contacts after aligning the V_{th} in panel (c), showing potential for sustaining performance while scaling contact length. (e) TLM structures of edge contacts with different contact length on the same 2L MoS_2 film. Scale bar, 1 μm. The 600 eV Ar ion beam exposure time is 5 s.

transfer length model (TLM) structures with different contact length on the same MoS_2 film (see inset of Figure 5e). Example I_d–V_{ds} curves of the TLM devices are plotted in Figure S17. The total resistances are obtained at n_{2D} = 1.2 × 10^{13} cm^2 and at small V_{ds} value of 0.54 V. The extracted contact resistances for edge contacts with L_c = 30 nm is ∼31 kΩ·μm, whereas for L_c = 80 nm, the contact resistance is slightly smaller at ∼30.5 kΩ·μm. This small difference between 30 and 80 nm contact length can be attributed to the slightly larger resistance of contact leads for shorter contact length (see Figure S18). The R_{tot} and R_c observed is 1 order of magnitude smaller than the best reported edge contacts in the literature (see comparison in Table S1). This improvement comes from the optimization of exposure time, the in situ UHV environment, and the transferred MoS_2 film.

Directly comparing these in situ edge-contacted 2D FETs with the other reported ex situ edge contacts can be difficult considering that parameters such as the carrier density, channel length, and film quality all need to be taken into account[30] (see Table S1). However, based on devices with similar carrier density and channel length, the in situ Ni edge contacts outperform the best-reported ex situ metal–MoS_2 edge contacts by an order of magnitude. This improvement could be associated with the different metal types, the directional ion beam etching and in situ metal deposition. Combined with the scaling result plotted in Figure 5c–e, the in situ Ni edge contacts demonstrate significant advances for better edge contacts to semiconducting 2D materials and show the ability for edge contacts to provide immunity to scaling in future scaled 2D FETs. Further work is needed to study contact lengths smaller than 20 nm, where the yield of metal contacts is low depending on the e-beam lithography tools and processes. As metal lines are scaled down to the width of single grains, other undesirable features begin to appear, such as ridges, valleys, and grain boundaries.[58] These effects will impact top contact performance more than edge contacts, as the top contact interfaces become nonsmooth, thus impacting the interfacial contact area. Research in this aspect remains scarce and merits further investigation.

One additional consideration is the resistance of scaled contact leads and their impact on device performance; the smaller the metal contact (in terms of L_c), the larger the resistance. We used two pads to connect each of the metal contacts in order to obtain the resistance of the contact leads, from the pads to the thin metal line (see Figure S18 for details). As L_c decreases from 80 to 20 nm, the resistance increases ∼30%, from 950 Ω to 1230 Ω. However, this resistance is far smaller than the total resistance of the device, thus its impact is negligible for the overall device performance. For future ultrascaled devices, where the contact resistance and the channel resistance have been reduced to a few hundred ohms, the resistance of the contact metal leads should be taken into account and studied explicitly.

Overall, while the top contacts can outperform in situ edge contacts at long contact lengths of L_c > 20 nm, attention should be given to the short contact length where the 2D materials would most likely be utilized in future scaled transistors. Furthermore, now that edge contacts to a 2D semiconductor have been demonstrated, continued study and optimization will improve their quality and resulting device performance. Further investigations may include (1) exploring more metal types to find a preferable edge interface; (2) doping the contact region before fabricating the edge contacts to further increase the number of carriers injected to the flake through the edge and thus decrease the contact resistance;[59] and (3) combining with shorter channel length to demonstrate edge-contacted, short-channel devices.

Conclusion. In situ edge contacts to MoS_2 FETs were demonstrated to provide immunity to contact length scaling for future generation devices. The challenge of preserving and utilizing the exposed, reactive edge of the MoS_2 was overcome by using *in situ* ion beam etching with contact metal deposition. The performance of the transistors remained consistent even as L_c ranged from 20 to 60 nm across a set of devices, experimentally demonstrating that edge contacts are advantageous for ultimate 2D contact scaling. Moreover, the comparison of edge contacts versus top contacts was demonstrated and the impact of different metals (Ni, Cr, and Au) was explored using the same edge contact scheme. Further theoretical and experimental investigations are warranted to better understand the edge contact interface and decrease the contact resistance. Our work sheds light on the potential of edge contacts for ultimate contact scaling in MoS_2 transistors and could be applied to other 2D materials and nanoelectronic devices, paving the road for future aggressively scaled devices.

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Methods. *CVD Growth of the MoS_2.* The MoS_2 flakes were grown using a chemical vapor deposition (CVD) process reported previously.[60−62] Typically, 1 g of sulfur powder (Sigma-Aldrich) and 15−30 mg of MoO_3 (99.99%, Sigma-Aldrich) source material were placed upstream and at the center of a tube furnace, respectively. The substrates (heavily doped Si substrate with 300 nm SiO_2) were placed downstream in the furnace tube. Typical growth was performed at 750 °C for 10 min under a flow of Ar gas in rate of 100 sccm and ambient pressure.

Fabrication of in Situ Edge-Contacted Devices. For devices using exfoliated flakes, multilayer MoS_2 flakes were mechanically exfoliated onto a heavily doped Si substrate with 300 nm SiO_2. For devices using CVD-grown MoS_2 films, the MoS_2 crystal was grown using the above process. For as-grown CVD MoS_2, the SiO_2 and the MoS_2 assembly coming out of the CVD furnace will be used for the subsequent device patterning. For transferred CVD MoS_2, an additional transfer process is needed.[57] EBL with PMMA was used to define the contact regions, leads, and pads. The substrate was then developed in a solution of IPA/MIBK= 3:1. After developing, the substrate was transferred to the UHV chamber (base pressure ≈ 10^{-8} Torr) having an ion beam source (KDC 40, KRI) in situ with an e-beam evaporator. The chip was exposed with a 600 eV directional Ar ion beam, followed by metal deposition. A top Au layer (30 nm) is also in situ deposited on top of the in situ Ni and Cr metal (normally 15 nm) to prevent oxidation of the contacts when exposed to ambient. This in situ ion beam process with metal deposition is crucial for protecting the exposed edges from other molecules in the ambient environment. Finally, the fabricated devices were characterized in dry N_2 after lift-off in acetone at a temperature of 80 °C.

Low-Temperature Measurement. The sample was loaded into Lakeshore probe station (CRX-6.5 K) and was cooled to base temperature (7 K) using a helium compressor (HC-4E1). The temperature was then increased gradually to 30, 50, 80, 140, 200, 250, and 300 K. The measurement was conducted at each temperature.

Characterization of the Edge Contact Interface. The AFM images in Figure 2 were taken from a Digital Instruments Dimension 3100. The SEM images are obtained using an FEI XL30 SEM-FEG. The EDS images in Figure 3 are obtained from a Bruker XFlash 4010 EDS. The cross-sectional STEM images in Figures 3 and 4 were prepared by using an FEI (Thermo-Fisher) Quanta 3D dual beam. A 250 nm coating of electron beam deposited Pt was deposited over the device followed by a 2 μm ion beam Pt deposition. Initial lift-out was performed with a 30 kV Ga beam, while final thinning was performed at 16 kV to reduce damage. The final polish of 48 pA at 5 kV was performed at ±4° to limit further damage. The STEM images were obtained using FEI Titan 80-300 probe aberration corrected STEM operated at 200 kV. The beam convergence angle was set to 20 mrad, and collection angles >50 mrad were used to obtain the Z-contrast high-angle annular dark-field (HAADF) images. The EDS images in Figures 3 and 4 were acquired from the SuperX system with the four Bruker Silicon Drift Detectors (SDD).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.9b01355.

Details on partial- and quasi-edge contacts to exfoliated multilayer MoS_2, low-temperature characterization of *in situ* Cr edge contacts, benchmarking of metal edge contacts, comparison of L_T and R_c component for top and edge contacts, cross-sectional images of MoS_2 with different etching time, and EDS mapping of individual element, comparison of various devices, and resistance of metal contacts with small L_c (PDF)

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Author Contributions

Z.C. and A.D.F. designed the experiments. Z.C. fabricated and characterized all the devices. Y.Y. grew the MoS_2 using CVD. S.S. helped characterize the devices. K.P. helped gather some early stage data. S.G.N. helped interpret the EDS data. Z.C. and A.F. wrote the main paper and the Supporting Information with input from all other authors.

Notes

The authors declare no competing financial interest.

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