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# Completely Printed, Flexible, Stable, and Hysteresis-Free Carbon Nanotube Thin-Film Transistors via Aerosol Jet Printing

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**Nanomaterials offer an attractive solution to the challenges faced for low-cost printed electronics, with applications ranging from additively manufactured sensors to wearables. This study reports hysteresis-free carbon nanotube thin-film transistor (CNT-TFTs) fabricated entirely using an aerosol jet printing technique; this includes the printing of all layers: semiconducting CNTs, metallic electrodes, and insulating gate dielectrics. It is shown that, under appropriate printing conditions, the gate dielectric ink can be reliably printed and yield negligible hysteresis and low threshold voltage in CNT-TFTs. Flexible CNT-TFTs on Kapton film demonstrate minimal variations in performance for over 1000 cycles of aggressive bending tests. New insights are also gained concerning the role of charge trapping in Si substrate-supported devices, where exposure to high substrate fields results in irreversible degradation. This work is a critical step forward as it enables a completely additive, maskless method to fully print CNT-TFTs of direct relevance for the burgeoning areas of flexible/foldable, wearable, and biointegrated electronics.**

Advances in materials science and manufacturing techniques are essential to the fabrication of robust, large-area, and low-cost printed electronics, which have attracted increasing attention for a broad variety of applications.[1–10] Some major challenges faced by printed electronics include the comparatively low carrier mobilities of many printed semiconductors, large channel lengths due to printing resolution limits, and poor switching behavior owing to the low quality or poor printability of gate insulators/dielectrics.[4,7,9,11–14] Single-walled carbon nanotubes (SWCNTs) have been intensely studied for use in thin-film transistors (TFTs) due to their excellent electronic,[15] thermal,[16] and mechanical[17] properties as well as their compatibility with solution-based processing.[5,12,18–23] One of the most promising aspects of CNT-TFTs is their compatibility with low-cost, high-throughput printing.[1,2,5,11] A broad range of applications in the realms of flexible electronics and Internet-of-Things, such as logic circuits,[21,24] display backplanes,[19] sensors,[8,25,26] and radiofrequency identification antennae,[27] would be made possible with low-cost printed CNT-TFTs.[4,25,28–30] However, several significant obstacles have limited the implementation and deployment of printed CNT-TFTs, including the large gate-induced hysteresis and associated temporal instabilities, the large threshold voltage ($V_{th}$), and the availability of reliable, printed dielectrics.[31,32]

Gate hysteresis in CNT-TFTs is mainly attributed to interface traps between the CNTs and the gate dielectric or other traps within the dielectric.[33] Hydroxyl groups (—OH) presented on oxide surfaces usually act as interface traps[32,34,35] while broken bonds within the amorphous oxide network are considered to be bulk defects that also serve as charge traps.[36,37] Although strategies to reduce the hysteresis, including high temperature annealing under vacuum,[32,33] encapsulation,[32,33] and surface treatment,[24,38] can be useful for certain cases, many of the materials and processes used are not compatible with a fully printed approach and in most cases only provide a partial solution that does not address both hysteresis and threshold voltage shift—a critical parameter for lowering power consumption.[6,31,39] Moreover, it remains technically challenging to print all layers of TFTs on both rigid and flexible substrates, largely due to the poor performance of printed interfaces, such as metal–semiconductor contacts,[11] or incompatibility of the inks/films with robust printing processes, in particular, for the gate dielectics.[4]

In fact, many of the reported "fully printed" TFTs (both CNT- and organic-TFTs) actually use nonprinting techniques to form some portion of the devices, such as photolithography for the source/drain (S/D) contacts[6,31] or, most commonly, immersing deposition of semiconducting CNTs for channels,[2,10] and spin-coating or vacuum deposition for the gate dielectrics.[21,30] There is one recent report, by Homenick et al., which utilizes a combination of roll-to-roll gravure printing and inkjet printing

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to fabricate fully printed SWCNT-based TFTs,[40] but nothing to date that uses a single printing system to fabricate the entire transistor. Recently, we have also made significant progress in the printing of metal contacts to printed CNTs, resulting in low contact resistance.[11] To our knowledge, there are only two kinds of printed dielectrics reported to date for printed CNT-TFTs: barium titanate/poly(methyl methacrylate) ($BaTiO_3$/PMMA)[2,12,40] and ion gels.[6,7,41] However, the performance, reliability, and surface morphology of nanoparticle–polymer dielectrics, like $BaTiO_3$/PMMA, highly depend on the size, shape, and spatial distribution of nanoparticles within the polymer matrix and the interaction and adhesion between the two phases.[42] It is also not favorable to incorporate barium compounds into the print process/devices. While exhibiting high capacitance, ion gel dielectrics are not stable at high temperature in air and limit the transistor speed and reliability.[12] Additionally, the CNT-TFTs with ion gel gate dielectrics exhibit ambipolar behavior, which often results in high leakage and static power consumption,[2,6] but may be used in certain special-case applications.[43,44] The same ambipolar problems are also encountered in polyfluorinated electrolyte based CNT-TFTs.[41] While poly(vinylphenol) (PVP)-based printed dielectrics have yielded good performance in organic transistors,[9,45] only one report can be found on the use of PVP in CNT-TFTs, with no mention of the hysteresis.[46] Thus, there are strong needs to explore alternative dielectrics with robust performance and printability and to develop practical fabrication processes for fully printed CNT-TFTs.

Here we report the printing of all layers of flexible, stable, and hysteresis-free CNT-TFTs via a single printing technology—aerosol jet printing. The active channel for the transistors was printed from high-purity (>99%) semiconducting CNTs while the electrodes were printed with Ag nanoparticle ink. A hydrophobic dielectric xdi-dcs—a blend of poly(vinylphenol)/poly(methyl silsesquioxane) (PVP/pMSSQ) was used for the printed gate dielectric. The xdi-dcs was recently shown to offer performance advantages for CNT-TFTs,[39] but only through spin-coating deposition. In this work, we make the dielectric ink truly compatible with fully printed electronics by demonstrating a properly tuned print process that retains the advantages of suppressed hysteresis and low threshold voltage. In the absence of encapsulation, both top- and bottom-gated fully printed devices showed little hysteresis and excellent temporal stability in transfer characteristics even under significant bias stress, which may be exploited in sensing applications. Compared with the bottom-gated CNT-TFTs in air ambient, the top-gated CNT-TFTs show a substantial reduction in threshold voltage and a more complete suppression of hysteresis. Furthermore, for Si substrate-supported devices, both the hysteresis and threshold voltage of the CNT-TFTs were significantly affected by applying a positive or negative voltage at the $SiO_2$ substrate gate, providing insight into the presence and role of charge traps at the $SiO_2$–CNT interface. The fully-printed CNT-TFT devices on Kapton films not only yield excellent performance, but also survive repeated aggressive bending tests over thousands of cycles with negligible change in electrical characteristics. A detailed study on the impact of various levels of strain is included, indicating the robustness of the devices in mechanically deformable form factors.

All layers in these CNT-TFTs were printed using an aerosol jet printer (AJ-300, Optomec Inc.).[11] Aerosol jet printing is capable of printing a variety of functional inks with line resolution down to ≈10 μm with either pneumatic or ultrasonic atomization.[6,7,11,47] The atomized ink is aerosolized in $N_2$ gas and fed out of a nozzle with an additional sheath of $N_2$ gas to circumvent clogging (Figure S1, Supporting Information). Considering the wide parameter space from atomization to relevant gas flows, nozzle size, and print speeds, aerosol jet printing provides one of the broadest ranges of controllable print variables among the various print process options, including inkjet, screen, and gravure printing.[11] **Figure 1**a schematically illustrates the main process involved in fabricating these fully printed CNT-TFTs on a rigid (p-doped Si wafer with 90 nm thick thermal $SiO_2$) or flexible (Kapton film) substrate. The substrate was first cleaned with acetone, isopropyl alcohol (IPA) and deionized (DI) water, followed by oxygen plasma (100 W) for 3 min. The surface was then functionalized by immersing into poly-L-lysine (PLL) solution (0.1% w/v in water; Sigma–Aldrich) for 5 min to enhance CNT adhesion to the $SiO_2$.[11,12,48] Note, in the case of the flexible Kapton substrates, the PLL step was not necessary for enhancing CNT adhesion. Silver (Ag) nanoparticle ink (Ag40X, UT Dot Inc.) was aerosol jet printed onto the substrates to define the patterns of the S/D electrodes. A postprinting sintering step at 150 °C for 60 min was carried out for the printed Ag electrodes to achieve better conductivity. Thereafter, for top-gated devices, thin-films of semiconducting CNTs (IsoSol-S100, Nanointegris Inc.) were aerosol jet printed as the channel regions. The samples were then rinsed by soaking for 30 s in toluene to remove excess surfactant followed by sintering in an oven at 150 °C for 30 min. Next, the dielectric ink (xdi-dcs, Xerox Research Center Canada) was printed onto the channel regions of the CNT-TFTs as the gate dielectric, followed by a two-step cure at 80 °C for 10 min and 140 °C for 30 min. Finally, Ag gate electrodes were printed and sintered to complete the fabrication of top-gated CNT-TFTs (Figure 1b). Figure S2 (Supporting Information) shows the optical images of the printed device after each layer was printed. The printed CNT-TFTs on Si wafers actually formed a dual-gate configuration: top-gated CNT-TFT with xdi-dcs as gate dielectric and substrate-gated CNT-TFT with $SiO_2$ as the gate dielectric. To fabricate flexible CNT-TFTs and circuity (Figure 1d), we used an ultrathin polyimide film (Kapton, DuPont, USA) with a thickness of 25 μm as the substrate. Typical channel length ($L$) and channel width ($W$) of such printed CNT-TFTs can be easily tuned in the range of 20–500 and 50–1000 μm, respectively. The parameters and details for printing each layer/material are summarized in the Experimental Section.

The morphologies of the as-printed, top-gated CNT-TFTs on rigid and flexible substrates are presented in Figure 1b–g, showing the dielectrics, CNT thin-film channel region, and Ag electrodes. An optical image of a representative top-gated CNT-TFT on Si is shown in Figure 1c, while an array of the CNT-TFTs on a flexible Kapton film is in Figure 1d. The scanning electron microscope (SEM) image of a representative CNT-TFT on Kapton is given in Figure 1e, in which the four different layers can be clearly seen. The SEM image in Figure 1f shows the uniform and high density semiconducting CNT thin-film network (≈40 CNTs $\mu m^{-2}$) in the channel region, which was

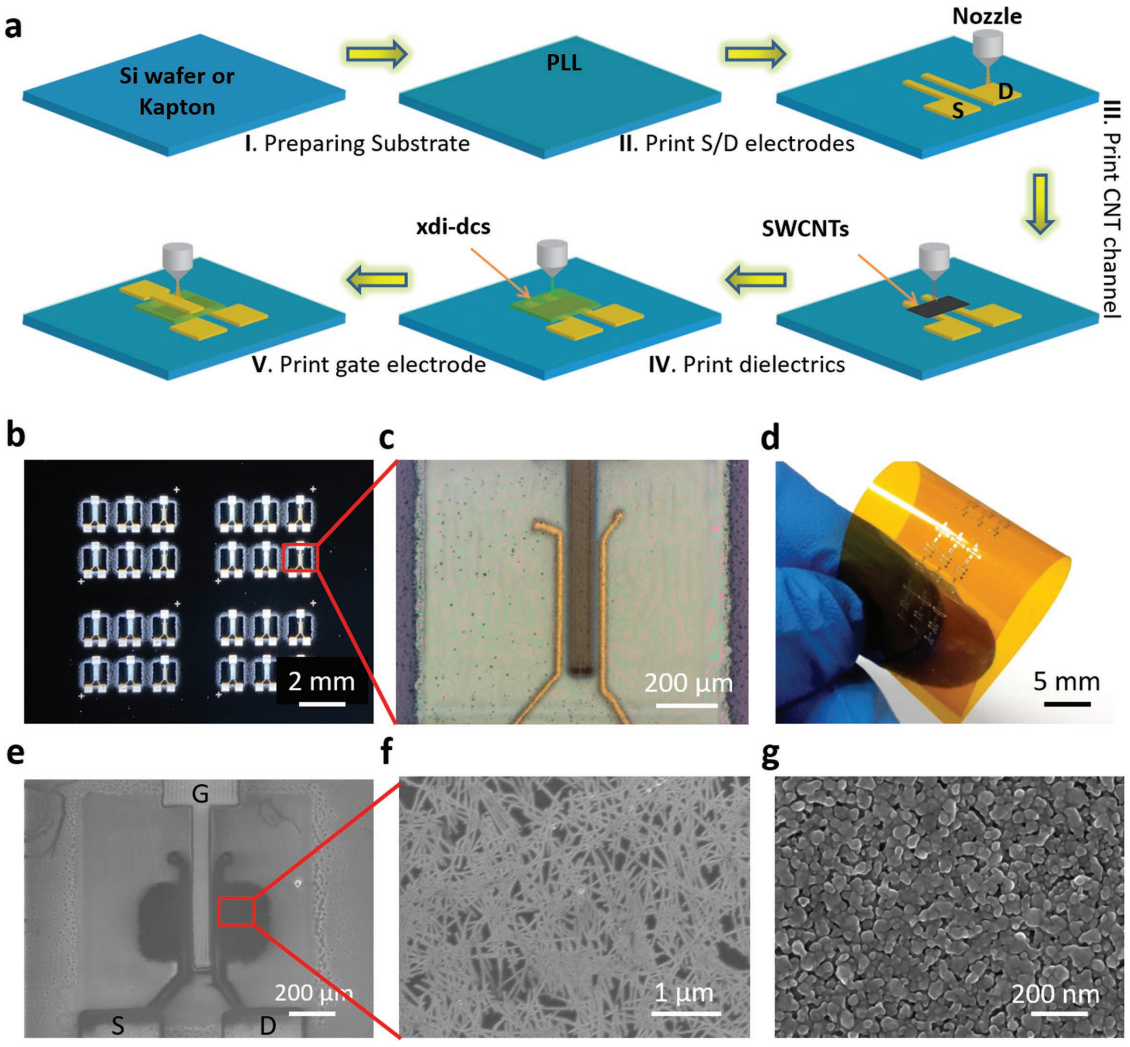


**Figure 1.** Fully-printed, flexible, and hysteresis-free carbon nanotube thin-film transistors (CNT-TFTs). a) Schematic diagram illustrating the fabrication process flow for top-gated CNT-TFTs, including (I) substrate preparation by cleaning, plasma treatment and modification with poly-L-lysine (PLL); aerosol jet printing of (II) source/drain electrodes, (III) CNT thin-film channel, (IV) gate dielectric, and (V) gate electrodes. b) Optical image of an array of printed CNT-TFTs on Si wafer. c) Optical image of a top-gated CNT-TFT after all layers are printed. d) Photograph of flexible CNT-TFTs and logic circuits on a Kapton film. e) Scanning electron microscope (SEM) image of top-gated CNT-TFT on Kapton with a clear view of the four printed layers including the underlying CNT network. f) SEM image of the semiconducting CNT network in the channel region of the CNT-TFT. The CNT network is uniformly distributed with a density of ≈40 CNTs $\mu m^{-2}$. g) SEM image of the printed Ag contact electrodes after sintering at 150 °C for 1 h. Ag nanoparticles have agglomerated to enhance conductivity.

printed with a sheath flow rate of 40 sccm, carrier flow rate of 23 sccm and speed of 2 mm $s^{-1}$. Figure 1g illustrates the morphology of the as-printed silver electrodes after sintering at 150 °C for 1 h, in which the Ag nanoparticles were partially merged together to give a good conductivity (sheet resistance < 20 Ω $sq^{-1}$). It should be noted that the ink properties, carrier flow rate, sheath flow rate, nozzle diameter, stage speed, and platen temperature were the main parameters adjusted for the optimization of each printed layer.

The gate dielectric (xdi-dcs), consisting of PVP and a low surface tension additive—pMSSQ,[39] was printed for the first time to get a uniform dielectric layer for both top- and bottom-gated CNT-TFTs. Compared to spin-coating, the printing method enables deposition of the dielectric to specific positions without coating the entire surface, thus leading to the preservation of ink (generating less waste), reduction of the number of processing steps (no need for patterned etch removal of the dielectric from other areas on the substrate), and more precise control of the thickness and morphology of the dielectric through tuning of the wide range of printing parameters. To determine the properties of the printed dielectric, parallel plate capacitors were fabricated as shown in Figure S3a (Supporting Information). Measuring the capacitance formed by the printed xdi-dcs layer and the $SiO_2$ (10 nm) in the metal oxide semiconductor structure yielded a dielectric constant of 3.85, as extracted from the plot of capacitance versus printed dielectric thickness (Figure S3b, Supporting Information). Details on the sample preparation and measurement are given in the Experimental Section and Figure S4 (Supporting Information). In addition, uniaxial tensile tests were conducted for thin xdi-dcs films with a

microstrain analyzer (MSA, TA Instruments RSA III) to obtain the stress–strain relationship and the shear modulus of the dielectric. As presented in Figure S5 (Supporting Information), the dielectric film exhibits a linear elastic behavior in the range of 5% strain. With the Neo-Hookean model, the shear modulus of the film is fitted as 45.2 MPa. When deposited onto the target substrates, this mixed dielectric material (PVP/pMSSQ) forms separate phases, with the pMSSQ migrating to the top to form a thin hydrophobic surface (Figure S3c, Supporting Information).[39] The water contact angle of the printed dielectric film was measured as 90.8°, which is slightly larger than that (84.3°) of the spin-coated xdi-dcs film, attributed to its larger surface roughness, as shown in the atomic force microscope (AFM) images of the printed and spin-coated xdi-dcs film on a silicon wafer in Figure S3d (Supporting Information). This enhanced hydrophobicity is beneficial to the application of the dielectric film in CNT-TFTs.[39] Furthermore, compared with the spin-coated xdi-dcs, the slightly rough surfaces of the printed films could improve the adhesion of CNTs in the bottom-gated CNT-TFTs. It is noted that the printed dielectric layer can be readily tuned from ≈800 nm to a few micrometers by changing printing parameters, such as number of print passes and the percentage of *n*-butanol. However, due to the larger thicknesses of the printed S/D and gate electrodes, a thicker printed dielectric layer better prevents electrical short between the gate electrode and the S/D electrodes and therefore makes the fabrication process more robust.

**Figure 2** presents the representative electrical characteristics of the fully-printed CNT-TFTs with xdi-dcs as gate dielectrics. Figure 2a,b shows the schematic configuration and optical image, respectively, of a representative top-gated CNT-TFTs on silicon. The channel length, $L$, and width, $W$, for the CNT-TFTs are $L = 120$ and $W = 200$ µm, respectively. The same dimensions and CNT configurations are used for all devices except those indicated otherwise. It can be seen from the subthreshold characteristics (Figure 2c) that the top-gated CNT-TFTs in ambient environment exhibit unipolar, p-channel operation with a negligible hysteresis (≈0.23 V) between forward (defined as $dV_{gs}/dt > 0$, where $d/dt$ is the time derivative and $V_{gs}$ is the gate voltage) and reverse ($dV_{gs}/dt < 0$) sweeps in gate–source voltage ($V_{gs}$).

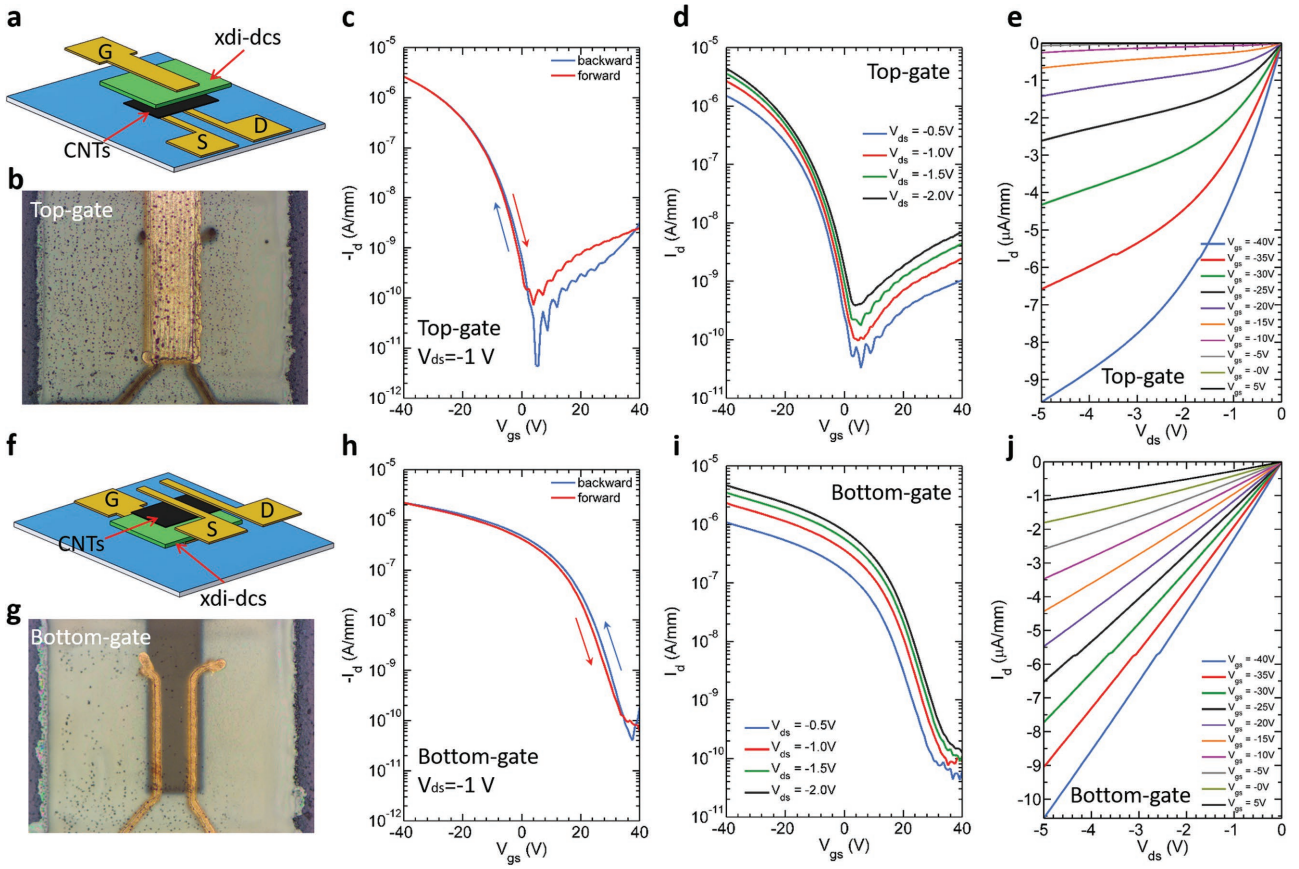


**Figure 2.** Performance and comparison of fully-printed, top- and bottom-gated CNT-TFTs on rigid substrates. a) Schematic of top-gated CNT-TFTs, with the layers vertically separated for clarity. b) Optical image of a representative top-gated device with the gate overlapping the source/drain contacts. c) Subthreshold characteristics ($I_d$–$V_{gs}$) of a top-gated device ($L = 120$ µm, $W = 200$ µm) with forward and reverse sweeps, measured with $V_{ds} = -1$ V, showing negligible hysteresis of ≈0.23 V and threshold voltage of −12.5 V. d) Subthreshold characteristics of the same device at different $V_{ds}$. e) Output characteristics ($I_d$–$V_{ds}$) of the same device, showing good saturation behavior at relatively low $V_{ds}$ for CNT-TFTs. f) Schematic of bottom-gated CNT-TFT, with the layers vertically separated for clarity. g) Optical image of a representative bottom-gated device with the gate overlapping the S/D electrodes. h) Subthreshold characteristics ($I_d$–$V_{gs}$) of a bottom-gated device ($L = 120$ µm, $W = 200$ µm) for forward and reverse sweeps, measured with $V_{ds} = -1$ V, showing small hysteresis of 2.4 V and threshold voltage of 2.3 V. i) Subthreshold characteristics ($I_d$–$V_{gs}$) of the same device measured at various $V_{ds}$. j) Output characteristics ($I_d$–$V_{ds}$) of the same device, indicating a good linear behavior in contacts.

Herein the magnitude of the hysteresis is defined as the difference between gate voltages needed to induce an average of the maximum and minimum drain current, i.e., $(I_{d,max}+I_{d,min})/2$, for the forward and reverse sweep directions.[31] The exceptionally small hysteresis in the present devices is in sharp contrast to the behavior of CNT-TFTs that use the substrate gate with 90 nm SiO2 layer as the dielectric (Figure S6, Supporting Information), wherein a large hysteresis of ≈35 V is present, due to charge trapping at the CNT–$SiO_2$ interface along with absorbed water molecules in the CNT films.[32,33]

The subthreshold characteristics in Figure 2d show the excellent ON/OFF current ratio ($I_{ON}/I_{OFF}$) of the top-gated CNT-TFTs at various drain–source voltages ($V_{ds}$), while the output characteristics in Figure 2e show the ON-state performance. The width-normalized ON-current ($I_{ON}/W$) of the device is calculated as 6.65 μA $mm^{-1}$ at $V_{ds} = -2.0$ V and $V_{gs} = -40$ V with an $I_{ON}/I_{OFF}$ of $\approx 6 \times 10^4$, which is consistent with other printed CNT-TFT devices and can be improved significantly upon further process optimization.[11] For example, the $I_{ON}/I_{OFF}$ increases with a reduced printed CNT density in the channel. Whenever the percolation threshold (≈12 tube $\mu m^{-2}$, calculated with Monte Carlo method) is smaller than the density of semiconducting CNTs but larger than that of the metallic CNTs, all percolation paths from source to drain will involve at least one semiconducting segment.[49,50] Field-effect mobility of the CNT-TFTs was calculated using the following expression: $\mu = (Lg_m)/(WC_{ox}V_{ds})$, where $L$ and $W$ are the device channel length and width, respectively, $g_m$ is the peak transconductance, $V_{ds} = -1$ V, and $C_{ox}$ is the gate capacitance per unit area as was calculated by a modified parallel-plate model discussed in previous work.[51] Based on the peak transconductance ($4.62 \times 10^{-8}$ S), extracted from the transfer curves in Figure 2c, the device mobility is ≈16.1 $cm^2$ ($V^{-1}$ $s^{-1}$), which is on par with other CNT-TFTs that have printed source/drain contacts and CNT channels.[1,10,23] The output characteristics ($I_d$–$V_{ds}$) of the same device exhibit clear current saturation that is typical for conventional field-effect transistors but rarely observed at such low $V_{ds}$ in TFTs, with a few exceptions.[24] Compared with top-gated CNT-TFTs with gate electrodes that did not overlap the source/drain contacts, we did not find any obvious enhancement in electrical performance with overlapping the gate electrodes on top of the S/D electrodes (Figure S7, Supporting Information), though there will obviously be a difference in the gate overlap capacitance. Figure S8 (Supporting Information) shows the subthreshold curves of 28 printed devices from different fabrication batches, indicating good yield and uniformity of the printing process.

With a reverse printing sequence (first printing the Ag gate electrode, then dielectric layer, CNTs and S/D electrodes), we also fabricated bottom-gated CNT-TFTs with the new printed gate dielectric (Figure 2f,g). As with the top-gated CNT-TFTs, the fully printed bottom-gated CNT-TFTs demonstrated negligible hysteresis (≈2.1 V over an 80 V sweep in $V_{gs}$), similar $I_{ON}$ and $I_{ON}/I_{OFF}$ (Figure 2h). However, the bottom-gated CNT-TFTs exhibit much larger threshold voltage $V_{th}$ = 2.3 V (Figure 2i) compared with the top-gated devices of −12.5 V (Figure 2d), which is attributed to the encapsulation effect of the PVP/pMSSQ xdi-dcs dielectric on the CNT channel in the top-gate design.[39] The top PVP/pMSSQ dielectric layer could also be eliminating electrostatic charge build up that can occur on exposed dielectric surfaces.[52] This is in contrast with other reports where encapsulation mainly draws water from the nanotube/dielectric interface. Under the same printing conditions for each layer, the slightly smaller $I_{ON}$ of the bottom-gated CNT-TFTs may be attributed to the lower adhesion between the hydrophobic dielectric polymers and the printed CNTs,[39] which may affect the final CNT density in the channel—something for further exploration in a follow-up study.

To further assess the quality of the printed xdi-dcs as a gate dielectric for printed CNT-TFTs, we performed a set of "stress test" measurements.[31,39] **Figure 3**a shows the transfer curves obtained at progressively greater top gate voltage ($V_{TG}$) sweep ranges. Compared to the previous report that showed strong bias-induced instability,[39] it is found that, at the measured ranges from ±10 to ±40 V, the hysteresis remains nearly constant and the threshold voltage ($V_{th}$) only slightly reduces with the increased bias stress. The inset in Figure 3a illustrates the $V_{th}$ for forward and reverse sweeps. The linear dependence of $V_{th}$ with $V_{TG}$ indicates a simple energy distribution of charge traps.[39,53] This signifies that only acceptor trap charges are responsible for the hysteresis and threshold shift.[39] The fully printed CNT-TFTs demonstrate extremely stable performance in ambient conditions. As shown in Figure 3b,c, the printed devices maintain stable hysteresis and threshold voltage ($V_{th}$) during the studying period of more than seven weeks. Additionally, the width-normalized ON-current ($I_{ON}/W$), ON/OFF current ratio ($I_{ON}/I_{OFF}$), and mobility ($\mu$) remain largely constant (Figure S9, Supporting Information). The device stability demonstrates that the printed xdi-dcs can serve as a favorable gate dielectric, yielding devices that are hysteresis-free and stable in air over an extensive amount of time.

Insights into the significant presence and nature of charge traps in the $SiO_2$ were obtained by studying top-gated CNT-TFTs that were subjected to various polarities of substrate-gate bias ($V_{BG}$) sweeps. Interestingly, the hysteresis and threshold voltage of the top-gated CNT-TFTs were dramatically affected by the swept $V_{BG}$, either positive or negative per the testing configuration. If a negative $V_{BG}$ sweep was applied ($0 \rightarrow -40$ V $\rightarrow 0$), and then the top-gated CNT-TFT retested ($I_d$–$V_{TG}$), then the ON-current, hysteresis, and $V_{th}$ will have been dramatically impacted. The $V_{th}$ of the top-gated CNT-TFTs is now shifted significantly and the $I_{ON}$ is radically reduced to less than 10% of its original value with a larger hysteresis (≈2.4 V) as seen in the third plot of Figure 3d. As time progresses, the performance of the device with the top-gate ($I_d$–$V_{TG}$) almost fully restores with respect to $I_{ON}$ and $I_{ON}/I_{OFF}$ within 10 min. Unfortunately, the final induced hysteresis (≈1.2 V) remains and cannot be completely eliminated. Meanwhile, the threshold voltage, taking the forward sweep as an example, is significantly shifted from $V_{th} = -21.6$ V initially to $V_{th} = -2.5$ V. This transformation in the $I_d$–$V_{TG}$ is reproducible by simply applying another negative $V_{BG}$ sweep, indicating that it is indeed related to charge traps in the $SiO_2$ and likely just beneath the $SiO_2$–CNT thin-film interface where the traps would have the most significant impact on the top-gate CNT-TFT performance. It is encouraging that these charge trapping effects do not present themselves when operating the printed CNT-TFT solely with the top-gate and printed dielectrics.

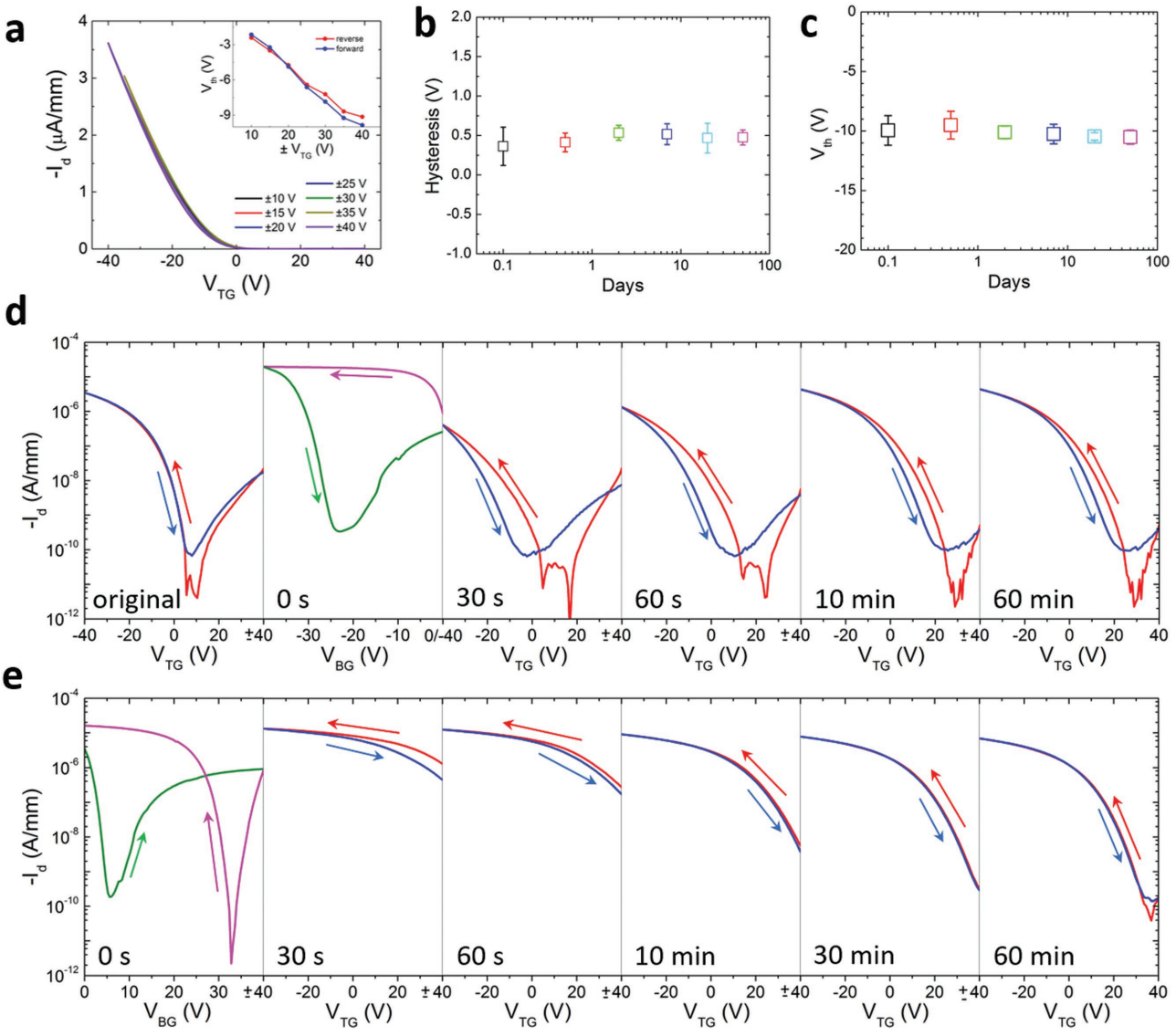


**Figure 3.** Stress test and substrate dielectric charge impact on CNT-TFTs. a) Gate dielectric stress test of the printed xdi-dcs dielectric with $V_{ds} = -1$ V, showing transfer curves at different sweep ranges from ±10 to ±40 V. Inset shows extracted threshold voltage ($V_{th}$) for forward and reverse sweep directions. b,c) Stability of hysteresis and threshold voltage ($V_{th}$) of the printed top-gated CNT-TFT devices in air ambient, measured at various times over 7 weeks. Each data point is averaged from 3 to 5 devices. d) Subthreshold characteristics ($I_d$–$V_{TG}$) of a top-gated CNT-TFT ($L = 120$ µm, $W = 200$ µm) before and after experiencing a negative gate voltage sweep ($I_d$–$V_{BG}$). The initial $I_d$–$V_{TG}$ hysteresis is only 0.3 V, but after applying a negative sweep ($0 \rightarrow -40$ V $\rightarrow 0$) from the substrate gate ($I_d$–$V_{BG}$), $I_{ON}$ in $I_d$–$V_{TG}$ dramatically drops, hysteresis increases to 2.4 V, and $V_{th}$ shifts to −21.6 V. In time, the $I_d$–$V_{TG}$ performance gradually restores, however, the hysteresis cannot be completely removed. The final hysteresis and threshold voltage are 1.2 and −2.5 V, respectively. e) Subthreshold characteristics ($I_d$–$V_{TG}$) of the same device after experiencing a positive sweep ($0 \rightarrow +40$ V $\rightarrow 0$) from the substrate gate ($I_d$–$V_{BG}$). The impact on $I_d$–$V_{TG}$ differs from the negative sweep case, as now $I_{ON}$ greatly increases, and hysteresis is subdued eventually to 0.8 V, while $V_{th}$ gradually shifts to 6.9 V after 1 h.

Comparatively, if a positive $V_{BG}$ sweep ($0 \rightarrow +40$ V $\rightarrow 0$) is applied and then the same top-gated CNT-TFT tested ($I_d$–$V_{TG}$) as shown in Figure 3e, the $I_{ON}$ will significantly increase to several times its original value, and a larger hysteresis (≈9.0 V) will arise. Moreover, $V_{th}$ becomes very large (≈48.6 V) and the $I_{ON}/I_{OFF}$ significantly degrades from $>10^4$ to <10. This result indicates that the applied positive $V_{BG}$ sweep has induced an opposite electrostatic doping effect in the CNT thin-film channel compared to the negative sweep. With time evolution shown in Figure 3e, $I_{ON}$ and $I_{ON}/I_{OFF}$ of the device can almost fully restore to their original values while the threshold voltage, which first dramatically shifted to 48.6 V, settles to 6.9 V and remains there permanently. In contrast to the case of applying a negative $V_{BG}$ sweep, the transistors experiencing the positive $V_{BG}$ sweep exhibit negligible hysteresis within ≈30 min. This phenomenon suggests that although the top-gated CNT-TFTs initially exhibit large negative $V_{th}$ and smaller $I_{ON}$, they can be greatly improved or tuned by applying an external electric field based on the charging of the supporting substrate oxide. Furthermore, with alternatively applying a positive or negative bias

at the back-gate (Figure 3d,e), the threshold voltage and hysteresis of the fully printed CNT-TFTs can be tuned on demand, which may be explored potentially as stable memory devices at room temperature.[37] A possible explanation to this phenomenon is that charging and discharging of the −OH groups in the channel region electrostatically modulate the semiconducting CNTs, thereby changing their conductivity. With a positive bias on the gate, −OH groups can trap electrons. The result is to shift the threshold voltage ($V_{th}$) of a p-type CNT-TFTs in the positive direction and to facilitate hole conduction during the forward gate voltage sweep. On the contrary, a negative gate bias discharges −OH groups into their neutral state, thereby reducing $V_{th}$ and the conductivity for hole transport during the reverse sweep.[33]

**Figure 4** describes the representative electrical characteristics and analysis of the impact of strain on fully printed CNT-TFTs on flexible substrates. An optical image of an array of top-gated CNT-TFTs printed on a Kapton film is shown in Figure 4a. The electrical characteristics of these devices were measured under different strain conditions based on the bending radius. First, the baseline configuration (prior to bending tests) of the devices is shown in Figure 4d–f. The subthreshold characteristics ($I_d$–$V_{gs}$) indicate negligible hysteresis (≈0.5 V) for the flexible CNT-TFTs, with a threshold voltage of −1.9 V. This demonstrates that the printed dielectrics can be used for fabricating flexible, hysteresis-free CNT-TFTs with small threshold voltage. The width-normalized on-current ($I_{ON}/W$) is ≈3.28 μA mm$^{-1}$, measured at $V_{ds}$ = −2 V. The average mobility of the devices was calculated in the same fashion as for those on the rigid Si substrates and found to be ≈4.1 cm$^2$ (V$^{-1}$ s$^{-1}$) while the $I_{ON}/I_{OFF}$ remains >10$^4$ on average. We also found that one-part xdi-dcs dielectric from Nanointegris Inc. can also give similar performance in the fully printed, flexible CNT-TFTs (Figure S10, Supporting Information). The frequency performance of the transistors may be limited by the printed dielectric and will be investigated in a future study.

The bending performance of the fully printed, flexible CNT-TFTs was tested, as illustrated in Figure 4j. A comparison of the transfer characteristics for a device measured after various numbers of bending cycles with a curvature radius of 1 mm is given in Figure 4g. The printed CNT-TFTs exhibit negligible variations in transfer characteristics down to a curvature radius of 1 mm even after 1000 cycles, indicating the excellent flexibility and reliability of the CNT-TFTs. It is found that there is no cracking or delamination observed on the Ag gate electrode (which is on top of the printed xdi-dcs dielectric) after 1000 bending cycles with a curvature radius of 1 mm (Figure 4b). Figure 4h shows the transfer characteristics of a CNT-TFT on Kapton measured while strained at various bending curvature radii. The slight differences in the characteristics between unstrained and bent to $r$ = 2 mm and $r$ = 1 mm are mainly due to the strains induced in the channel region and the interfaces between contact materials. It is also found that the gate leakage current exhibits no perceptible change when the substrate is bent to different radii of curvature (see Figure S11 in the Supporting Information).

Finite element modeling was used to study the variations of this tensile strain at the top surface of the printed dielectric film as a function of the bending radius (Figure S12, Supporting Information). The tensile strain on top of the printed dielectric layer (xdi-dcs film) increases with reduction of the bending radius $r$ for a given substrate thickness,[54] and for a specific bending radius, the tensile strain decreases with reduction of the thickness of substrate, as shown in Figure 4i. Therefore, adopting an ultrathin substrate will substantially reduce the induced strains for highly flexible electronics.[28,30] The strain distribution of the bent dielectric film under different curvature radii is shown in Figure 4j, in which the substrate is 25 μm thick. When bending with a radius of $r$ = 1, 2, or 5 mm in the experimental study, no damage is observed on the electrodes. However, when the bending radius decreases down to $r$ = 0.5 mm, the maximum tensile strain on the top surface can reach up to ≈3.51%, resulting in partial delamination and cracking of the Ag gate electrodes (Figure 4c). Using a thinner substrate film of 10 μm thick, the maximum strains at the top of the dielectric film will be 2.12% when bending to a curvature radius of 0.5 mm (Figure 4i), similar to the strain level of the 25 μm thick substrate under the radius of 1 mm, which indicates that the flexible CNT-TFTs on the 10 μm substrate can survive when bending to a curvature of $r$ = 0.5 mm. The delamination and cracks that occurred in the Ag electrodes are the primary reason for the device failure and performance degradation under the more extreme strains. Hence, the robustness to extreme strain (flexibility) will be greatly improved by adopting more compliant electrodes, such as silver nanowires or metallic carbon nanotubes, where were demonstrated in our recent work.[11,26,55]

To compare the performance of the printed, flexible CNT-TFTs with xdi-dcs (PVP/pMSSQ) as the gate dielectric from this work with other printed CNT-TFTs that use different dielectrics (PVP/pMSSQ, $BaTiO_3$, ion gel, and Teflon-AF) in the literature,[2,6,12,39,56] a summary of key metrics is given in **Figure 5** and Table S1 (Supporting Information). Except the spin-coated PVP/pMSSQ by Lefebvre et al.,[39] all other devices in Figure 5 used printed dielectrics with a diversity of printing techniques. With respect to hysteresis (≈0.5 V) and threshold voltage (≈−1.9 V), the completely printed devices in this work demonstrated competitive performance with the devices that use spin-coated PVP/pMSSQ. The CNT-TFTs in this work yielded better performance than the CNT-TFTs with printed $BaTiO_3$, which exhibit sizable hysteresis. In fact, these fully printed CNT-TFTs with the printed xdi-dcs dielectric perform on par with the partially printed ion gel CNT-TFTs. This is a substantial accomplishment considering the operation of ion gels, which essentially act as extremely thin dielectrics due to ionic charge migration throughout. The extremely large ON-current in the partially printed devices with the ion gel gate is largely attributed to the much smaller channel length (10 μm) from their use of photolithographic patterning rather than printing to form the contacts.

In summary, we have demonstrated flexible, stable, and hysteresis-free CNT-TFTs that were fabricated by the aerosol jet printing of all layers—truly fully printed CNT-TFTs. The printed xdi-dcs gate dielectric is the first to show negligible hysteresis with excellent stability in the transfer characteristics even under significant bias stress, and a threshold voltage consistently smaller than other CNT-TFTs, including those that are Si substrate gated. A comparison of top- and bottom-gated printed CNT-TFTs with this new approach revealed a considerable difference in ON- and OFF-state performance, with the top-gated

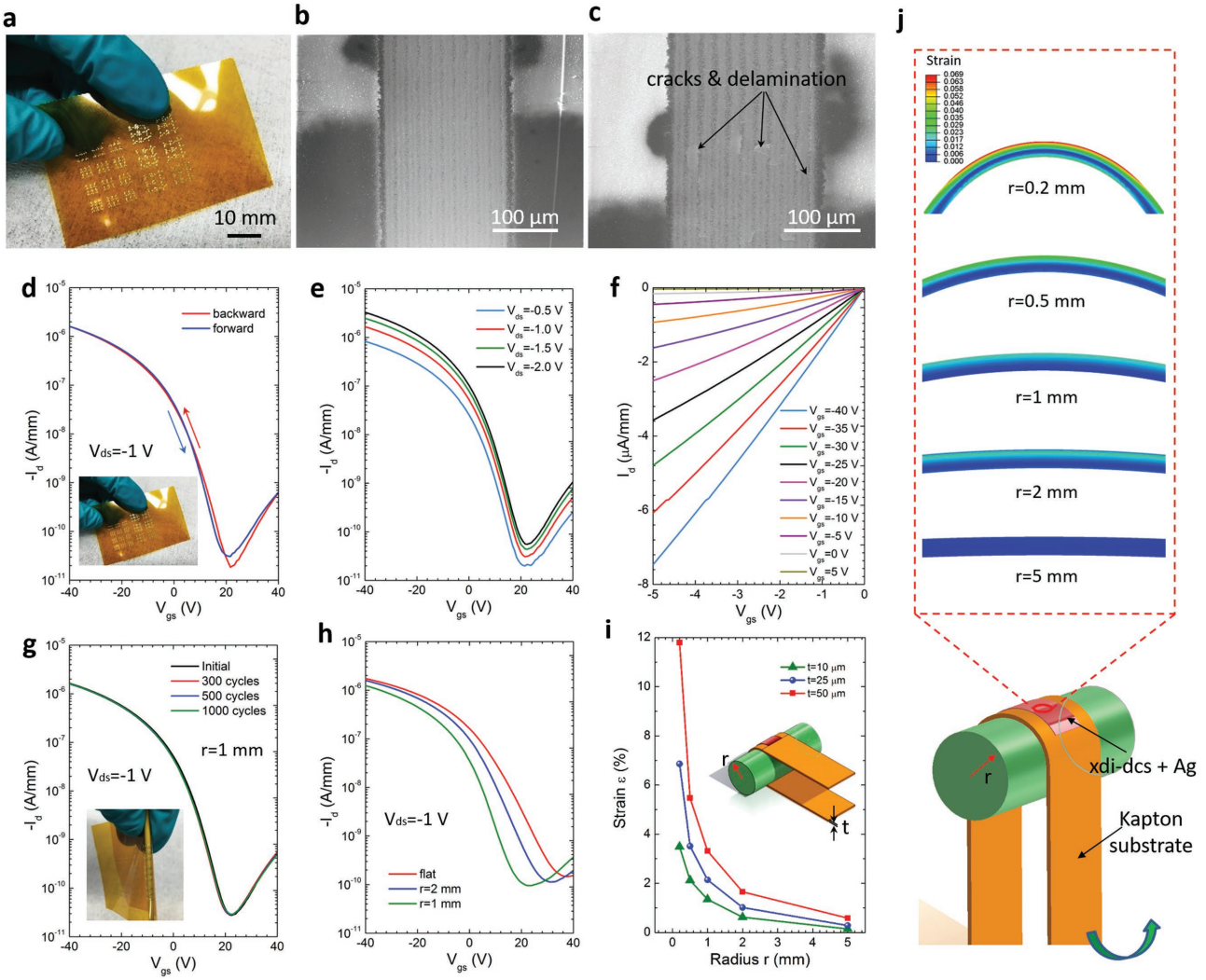


**Figure 4.** Performance and bending tests of fully-printed CNT-TFTs on flexible substrates. a) Photograph of fully-printed, top-gated CNT-TFT arrays on a Kapton film (25 µm thick). b) SEM image of the Ag gate electrode after 1000 bending cycles with a radius of curvature 1 mm—there are no cracks or delamination observed on the electrode. c) SEM image of the Ag gate electrode after multiple bending cycles with a radius of curvature 0.5 mm, resulting in partial delamination and cracks at some points in the electrode. d) Subthreshold characteristics ($I_d$–$V_{gs}$) of a representative top-gated CNT-TFT ($L$ = 120 µm, $W$ = 200 µm) measured for forward and reverse sweeps with negligible hysteresis of ≈0.5 V and threshold voltage of –1.9 V. e) Subthreshold and f) output characteristics of the same device. g) Subthreshold characteristics of a device measured after various numbers of bending cycles with a curvature radius of 1 mm and h) at various bending curvature radii. The Kapton film is 25 µm thick. Insets of (g): Photograph of the printed device substrate being wrapped around a cylinder with a curvature radius of 1 mm. Device performance varied negligibly when bent down to a curvature radius of 1 mm over 1000 cycles. i) Variation of the tensile strains on top of the dielectric film printed on a flexible substrate as a function of bending radius. The tensile strain increases with the substrate thickness and reduces with the bending radius. j) Strain distribution of the bent dielectric film on top of a Kapton substrate (25 µm thick), calculated from finite element models. Higher tensile strains occur on the top surface of the xdi-dcs film when bent to a smaller radius.

devices yielding higher currents and better switching behavior. We also demonstrated that these fully printed CNT-TFTs are readily compatible with flexible substrates, whereon they show negligible change in electrical characteristics after over thousands of cycles of aggressive bending. These new findings for fully printed CNT-TFTs provide important advancement in fabricating all-layer printed, flexible and low-cost CNT-TFTs via an additive and maskless method, which paves the way towards developing practical applications of all-printed CNT-TFTs in emerging electronics such as wearable, foldable, and biointegrated devices.

## Experimental Section

*Substrate Cleaning*: The silicon wafers or Kapton films were rinsed with DI water for 1 min, and further sonicated in acetone and IPA for 10 min each (25 °C) and blown dry with $N_2$ gas. The wafers were subsequently subjected to 3 min of oxygen ($O_2$) plasma (Emitech K-1050X) at 100 W under vacuum (0.6 Torr).[11]

*Functionalization of Si Wafer*: Prior to CNT channel printing, the cleaned wafer was immersed into PLL solution (0.1% w/v in water; Sigma–Aldrich) for 5 min to functionalize the $SiO_2$ surface for increasing the adhesion between printed CNTs network and substrate. The functionalized wafer was then rinsed with DI water to remove the unattached monomers, and blown dry thoroughly using $N_2$ gas.

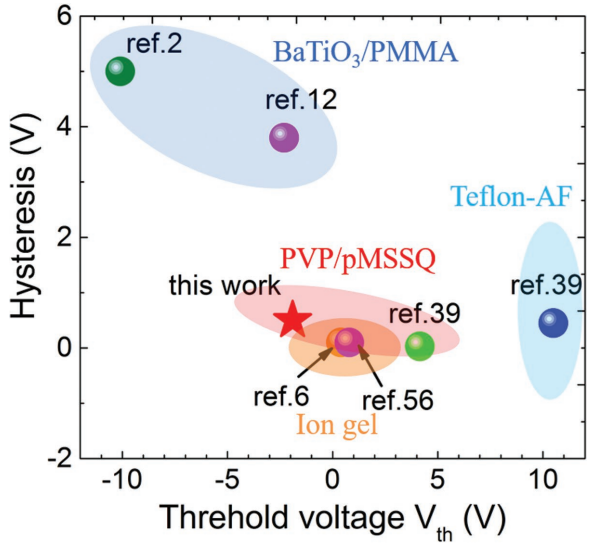


**Figure 5.** Performance (hysteresis and threshold voltage) comparison of the completely printed, flexible CNT-TFTs with other printed CNT-TFTs in literature. The star indicates the performance of printed flexible devices in this work, with a hysteresis of ≈0.5 V and a threshold voltage of −1.9 V. Four different kinds of dielectrics are shown, indicated with the ellipses: PVP/pMSSQ or xdi.dcs (red), $BaTiO_3$/PMMA (blue), ion gel (orange), and Teflon-AF (cyan). Dielectrics in ref. [39] were spin-coated while the devices in ref. [2] and ref. [6] are partially printed. Extraction from referenced studies was approximated from reported curves if not explicitly provided.

*Printing Ag Electrodes*: The Ag ink (Ag40X, UT Dots Inc.) contained 40 wt% Ag nanoparticles, with particle diameters ≈20 nm, dispersed in a solvent mixture of xylene and terpineol (9:1 by volume). The prepared ink was printed on $SiO_2$/Si substrates. A 100 µm diameter nozzle was used for printing, and the flow rates of sheath gas and carrier gas were set to 25 and 15 sccm, respectively. The temperature of chilling water bath was kept at 15 °C and platen temperature was set to 60 °C. The printed samples were further sintered at 150 °C in air for 60 min in an oven (MDL 281, Fisher Scientific Co.) to enhance the conductivity.

*Printing CNT Channels*: The semiconducting CNT ink (IsoSol-S100, Nanointegris Inc.) with a purity of 99% semiconducting single-walled CNTs and a concentration of 0.05 mg $mL^{-1}$ was purchased from Nanointegris Inc., Canada. It was further diluted with toluene to 0.01 mg $mL^{-1}$ for aerosol jet printing. The as-prepared CNT ink was printed using a 150 µm diameter nozzle, and the sheath and carrier gas flow rates were 40 and 23 sccm, respectively. The printing speed was fixed at 2 mm $s^{-1}$. The water bath for ink vials was kept at 20 °C. All printing was carried out in air at room temperature while platen was maintained at 60 °C to accelerate ink drying. After printing, the samples were rinsed with toluene to remove excess surfactant followed by sintering in air ambient at 150 °C for 30 min.

*Printing Dielectric*: The two-part dielectric ink (xdi-dcs), consisting of PVP and pMSSQ, was obtained from Xerox Research Center Canada. The dielectric ink was formed by mixing the two components: poly(vinylphenol) and poly(methyl silsesquioxane) in a ratio of 10:1, and then diluted with four times of *n*-butanol to a lower viscosity for ultrasonication atomization. For the one-part dielectric ink from Nanointegris Inc., twice amount of *n*-butanol was added for tuning the viscosity. A nozzle of 150 µm diameter was used for printing, and the sheath flow and carrier flow were set to 20 and 28 sccm, respectively. The printing speed ranged from 5 to 10 mm $s^{-1}$ depending on the targeted thickness of the dielectrics. The temperature of chilling water bath was kept at 20 °C and platen temperature was set to 30 °C. The as-printed samples were postcured at 80 °C for 10 min on a hotplate and then at 140 °C for 30 min in an oven (MDL 281, Fisher Scientific Co.).

*Measurement of the Contact Angles of Dielectric Films*: The static contact angles of the samples were measured using a Ramé-Hart goniometer equipped with a dispensing needle and all the tests were performed in air at ambient temperature. A sessile drop (DI water) of 5 µL was generated by the automatic dispensing needle. After measurement, the water drops were gently removed by compressed air to dry the film surface for repeated contact angle testing. The reported values in the figure were the mean values of five different measurements from a same sample.

*Capacitance–Voltage (C–V) Measurements of Gate Dielectric*: The permittivity (dielectric constant) of the xdi-dcs was determined from *C–V* measurements of the parallel capacitors formed by the thin layers of $SiO_2$ and xdi-dcs. Three different sizes of the capacitors were fabricated by printing different thicknesses of xdi-dcs on a p-doped Si wafer with 10 nm of thermal $SiO_2$ (Figure S4, Supporting Information). The top electrodes of the capacitors were deposited on top of the dielectric layers to form a parallel-plate capacitance. The *C–V* measurements were performed using an Agilent (Keysight Technologies) B1500A Semiconductor Parameter Analyzer connected to a Lakeshore CRX 6.5K cryogenic probe station. For each capacitor, three *C–V* measurements were carried out under three different frequencies: 1 kHz, 100 kHz, and 1 MHz. The capacitance of the dielectric film was calculated using the equation for parallel capacitor in Figure S3b (Supporting Information), and used to fit the permittivity of the dielectric material.

*Characterizations of Printed CNT-TFTs*: Optical images of devices were taken by a Zeiss Axio Lab microscope configured with 2.5× to 100× objective lenses and a digital camera for image capture and analysis. SEM images of printing patterns and devices were acquired with FEI XL30 (SEM-FEG, USA) with varied magnifications and beam conditions. AFM images of dielectric films were taken with a Dimension 3000 instrument in tapping mode. The film thickness is measured by a profilometer (Bruker Dektak 150). Electrical characterization of the printed CNT-TFTs was carried out in air using a Lakeshore probe station (Lakeshore CRX-6.5K) along with an Agilent B-1500 Semiconductor Parameter Analyzer. The sheet resistance was measured with four probe methods using a Keithley 2400 and 236 source measuring units.

*Mechanical Testing of xdi-dcs Film*: The tensile tests were conducted with a microstrain analyzer (MSA, TA Instruments RSA III). Xdi-dcs was casted into a Petri dish covered with a layer of aluminum foil for easily detaching. After curing at a hotplate at 80 °C for 1 h and in an oven at 140 °C for 1 h, the final film was peeled off from the foil and cut into small strips. In measurement, the strips were gripped using film tension clamps with a clamp compliance of ≈0.3 µm $N^{-1}$. All tensile tests were conducted in a controlled strain mode with a preload of 0.01 N and a strain ramp of 0.05% $min^{-1}$ unless otherwise specified. The width and thickness of the samples were measured using a digital caliper. The length between the clamps was automatically measured and recorded by the MSA.

*Finite Element Modeling of Bending Test*: The printed dielectric on flexible Kapton films was modeled with the CPE4R elements under plane-strain deformation using the FEM software package, ABAQUS. The Neo-Hookean material model is used for the xdi-dcs and the Kapton. The cylinder for bending test is set as a rigid body. In the simulation, displacement loadings were applied to control the bending of the film. Mesh convergence for the model was performed to ensure the accuracy of the results.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

aerosol jet printing, carbon nanotubes, gate dielectrics, printed flexible electronics, thin-film transistors

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