

# Aaron D. Franklin

## Curriculum Vita

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### Education

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Ph.D. Electrical Engineering	<b>Purdue University</b> West Lafayette, IN	2008
B.S. Electrical Engineering Minor: Communication	<b>Arizona State University</b> Tempe, AZ	2004

### Honors and Awards

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- Bass Chair & Fellow of Bass Society at Duke 2018
  - Best Paper Award (*advisor*) at international IEEE Sensors conference 2017
  - 2<sup>nd</sup> Place at MRS iMatSci Innovation Showcase for Tire Tread Wear Sensor Technology 2017
  - Best Poster Award (*advisor*) at Device Research Conference (DRC) 2017
  - IBM Labyrinth Award for Invention Accomplishments 2014
  - IBM Outstanding Technical Achievement Award 2014
  - IBM Research Outstanding Contributor Award 2013
  - GOMAC Technology Conference #1 Outstanding Paper Award 2012
  - IBM Invention Achievement Awards 2009, 2011, 2012, 2013
  - GOMAC Technology Conference Meritorious Paper Award 2010
  - National Science Foundation (NSF) Graduate Research Fellowship (GRF) 2005 - 2008
  - First place poster prize and NSF travel scholarship for Nano and Giga Conference 2007
  - Materials Research Society (MRS) Graduate Student Silver Award 2006
  - NASA Institute for Nanoelectronics and Computing (INaC) Fellowship 2005 - 2006
  - Purdue University Andrews Recruiting Fellowship 2005 - 2006
  - Graduate of Barrett Honors College at Arizona State University 2004
  - Arizona State University Distinguished Electrical Engineering Senior of the Year Award 2004
  - Fifteen top-ranking awards in persuasive, informative, and impromptu speaking and debate at various Intercollegiate Speech and Debate tournaments 2001 - 2002

### Academic and Professional Appointments

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<b>Co-Founder &amp; Chief Technology Officer (CTO)</b> <i>Tyrata, Inc.</i>	2017 - Present
<b>James L. and Elizabeth M. Vincent Associate Professor</b> <i>Duke University, Department of Electrical and Computer Engineering (ECE)</i>	2018 - Present
<b>Director of Graduate Studies</b> <i>Duke University, Department of Electrical and Computer Engineering (ECE)</i>	2017 - Present
<b>Associate Professor</b> <i>Duke University, Department of Electrical and Computer Engineering (ECE) &amp; Department of Chemistry</i>	2014 - Present
<b>Adjunct Assistant Professor</b> <i>Columbia University, Department of Electrical Engineering</i>	2013 - 2014
<b>Research Staff Member</b> <i>IBM, T. J. Watson Research Center, Physical Science and Silicon Departments</i>	2008 - 2014
<b>NSF Graduate Research Fellow</b> <i>Purdue University, School of Electrical and Computer Engineering</i>	2004 - 2008

### Publications (h-index = 30)

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1. J. B. Andrews, J. A. Cardenas, C. J. Lim, S. G. Noyce, J. Mullett, and A. D. Franklin, "Fully printed and flexible carbon nanotube transistors for pressure sensing in automobile tires," *IEEE Sensors Journal*, (in press).
  2. J. B. Andrews, K. Mondal, T. Neumann, J. A. Cardenas, J. Wang, D. P. Parekh, Y. Lin, P. Ballentine, M. D. Dickey, and A. D. Franklin, "Patterned liquid metal contacts for printed carbon nanotube transistors," *ACS Nano*, vol. 12, pp. 5482-5488, 2018.

3. J. A. Cardenas, M. J. Catennaci, J. B. Andrews, N. X. Williams, B. J. Wiley, and **A. D. Franklin**, "In-place printing of carbon nanotube transistors at low temperature," *ACS Appl. Nano Mater.*, vol. 1, pp. 1863-1869, 2018.
4. S. Najmaei, M. R. Neupane, B. M. Nichols, R. A. Burke, A. L. Mazzoni, M. L. Chin, D. A. Rhodes, L. Balicas, **A. D. Franklin**, and M. Dubey, "Cross-plane carrier transport in van der Waals layered materials," *Small*, vol. 14, pp. 1703808, 2018.
5. **A. D. Franklin**, D. Jena, and D. Akinwande, "75 years of the Device Research Conference – A history worth repeating," *IEEE J. Electron Devices Society*, vol. 6, pp. 116-120, 2018.
6. Y. -C. Lin, F. A. McGuire, and **A. D. Franklin**, "Realizing ferroelectric  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  with elemental capping layers," *J. Vac. Sci. Technol. B*, vol. 36, pp. 011204, 2018.
7. Q. Han, Y. Bai, J. Liu, K. Du, T. Li, D. Ji, Y. Zhou, C. Cao, D. Shin, J. Ding, **A. D. Franklin**, J. T. Glass, J. Hu, M. J. Therien, J. Liu, and D. B. Mitzi, "Additive engineering for high-performance room-temperature-processed perovskite absorbers with micron-size grains and microsecond-range carrier lifetimes," *Energy & Environmental Sci.*, vol. 10, pp. 2365-2371, 2017.
8. F. A. McGuire, Y. -C. Lin, K. Price, G. B. Rayner, S. Khandelwal, S. Salahuddin, and **A. D. Franklin**, "Sustained sub-60 mV/decade switching via the negative capacitance effect in  $\text{MoS}_2$  transistors," *Nano Lett.*, vol. 17, pp. 4801-4806, 2017.
9. K. M. Price, K. E. Schauble, F. A. McGuire, D. B. Farmer, and **A. D. Franklin**, "Uniform growth of sub-5 nm high- $\kappa$  dielectrics on  $\text{MoS}_2$  using plasma-enhanced atomic layer deposition," *ACS Appl. Mater. Interfaces*, vol. 9, pp. 23072-23080, 2017.
10. J. B. Andrews, C. Cao, M. Brooke, and **A. D. Franklin**, "Noninvasive material thickness detection by aerosol jet printed sensors enhanced through metallic carbon nanotube ink," *IEEE Sensors Journal*, vol. 17, pp. 4612-4618, 2017.
11. C. Cao, J. B. Andrews, and **A. D. Franklin**, "Completely printed, flexible, stable, and hysteresis-free carbon nanotube thin-film transistors," *Adv. Electronic Mater.*, vol. 3, pp. 1700057, 2017.
12. M. J. Catenacci, P. F. Flowers, C. Cao, J. B. Andrews, **A. D. Franklin**, and B. J. Wiley, "Fully printed memristors from  $\text{Cu-SiO}_2$  core-shell nanowire composites," *J. Electronic Mater.*, 2017.
13. N. D. Cox, C. D. Cress, J. E. Rossi, I. Puchades, A. Merrill, **A. D. Franklin**, and B. J. Landi, "Modification of silver/single-wall carbon nanotube electrical contact interfaces via ion irradiation," *ACS Appl. Mater. Interfaces*, vol. 9, pp. 7406-7411, 2017.
14. D. Joh, F. McGuire, R. Abedini-Nassab, J. Andrews, R. Achar, Z. Zimmers, D. Mozhdehi, R. Blair, F. Albarghouthi, W. Oles, J. Richter, C. Fontes, A. Hucknall, B. Yellen, **A. D. Franklin**, and A. Chilkoti, "Poly(oligo(ethylene glycol) methyl ether methacrylate) brushes on high- $\kappa$  metal oxide dielectric surfaces for bioelectrical environments," *ACS Appl. Mater. Interfaces*, vol. 9, pp. 5522-5529, 2017.
15. S. Najmaei, S. Lei, R. Burke, B. M. Nichols, A. George, P. M. Ajayan, **A. D. Franklin**, J. Lou, and M. Dubey, "Enabling ultra-sensitive photo-detection through control of interface properties in molybdenum disulfide atomic layers," *Sci. Rep.*, vol. 6, pp. 39465, 2016.
16. F. A. McGuire, Z. Cheng, K. Price, and **A. D. Franklin**, "Sub-60 mV/decade switching in 2D negative capacitance field-effect transistors with integrated ferroelectric polymer," *Appl. Phys. Lett.*, vol. 109, pp. 093101, 2016.
17. Z. Cheng, J. A. Cardenas, F. A. McGuire, S. Najmaei, and **A. D. Franklin**, "Modifying the Ni- $\text{MoS}_2$  contact interface using a broad-beam ion source," *IEEE Electron Device Lett.*, vol. 37, pp. 1234-1237, 2016.
18. C. Cao, J. B. Andrews, A. Kumar, and **A. D. Franklin**, "Improving contact interfaces in fully printed carbon nanotube thin-film transistors," *ACS Nano*, vol. 10, pp. 5221-5229, 2016.
19. **A. D. Franklin**, "Nanomaterials in transistors—from high-performance to thin-film applications," *Science*, vol. 349, pp. aab2750, 2015.
20. J. Li, **A. D. Franklin**, and J. Liu, "Gate-free electrical breakdown of metallic pathways in single-walled carbon nanotube crossbar networks," *Nano Lett.*, vol. 15, pp. 6058-6065, 2015.
21. Q. Cao, S. -J. Han, J. Tersoff, **A. D. Franklin**, Y. Zhu, Z. Zhang, G. S. Tulevski, J. Tang, and W. Haensch, "End-bonded contacts for carbon nanotube transistors with low, size-independent resistance," *Science*, vol. 350, pp. 68-72, 2015.

22. C. -S. Lee, E. Pop, **A. D. Franklin**, W. Haensch, and H. -S. P. Wong, "A compact virtual-source model for carbon nanotube field-effect transistors in the sub-10-nm regime—Part II: Extrinsic elements, performance assessment, and design optimization," *IEEE Trans. Electron Devices*, vol. 62, pp. 3070-3078, 2015.
23. C. -S. Lee, E. Pop, **A. D. Franklin**, W. Haensch, and H. -S. P. Wong, "A compact virtual-source model for carbon nanotube field-effect transistors in the sub-10-nm regime—Part I: Intrinsic elements," *IEEE Trans. Electron Devices*, vol. 62, pp. 3061-3069, 2015.
24. G. S. Tulevski, **A. D. Franklin**, D. Frank, J. M. Lobeze, Q. Cao, H. Park, A. Afzali, S. -J. Han, J. B. Hannon, and W. Haensch, "Toward high-performance digital logic technology with carbon nanotubes," *ACS Nano*, vol. 8, pp. 8730-8745, 2014.
25. **A. D. Franklin**, D. B. Farmer, and W. Haensch, "Defining and overcoming the contact resistance challenge in scaled carbon nanotube transistors," *ACS Nano*, vol. 8, pp. 7333-7339, 2014.
26. B. Kim, **A. D. Franklin**, C. Nuckolls, W. Haensch, and G. S. Tulevski, "Achieving low-voltage thin-film transistors using carbon nanotubes," *Appl. Phys. Lett.*, vol. 105, pp. 063111, 2014.
27. D. Shahrjerdi, **A. D. Franklin**, S. Oida, J. A. Ott, G. S. Tulevski, and W. Haensch, "High-performance air-stable n-type carbon nanotube transistors with erbium contacts," *ACS Nano*, vol. 7, pp. 8303-8308, 2013.
28. **A. D. Franklin**, "The road to carbon nanotube transistors," *Nature*, vol. 498, pp. 443-444, 2013.
29. **A. D. Franklin**, S. O. Koswatta, D. B. Farmer, J. T. Smith, L. Gignac, C. M. Breslin, S. -J. Han, G. S. Tulevski, H. Miyazoe, W. Haensch, and J. Tersoff, "Carbon nanotube complementary wrap-gate transistors," *Nano Lett.*, vol. 13, pp. 2490-2495, 2013.
30. J. Luo, L. Wei, C. -S. Lee, **A. D. Franklin**, X. Guan, E. Pop, D. A. Antoniadis, and H. -S. P. Wong, "A compact model for carbon nanotube field-effect transistors including non-idealities and calibrated with experimental data down to 9 nm gate length," *IEEE Trans. Electron Devices*, vol. 60, pp. 1834-1843, 2013.
31. J. T. Smith, **A. D. Franklin**, D. B. Farmer, and C. Dimitrakopoulos, "Reducing contact resistance in graphene devices through contact area patterning," *ACS Nano*, vol. 7, pp. 3661-3667, 2013.
32. G. S. Tulevski, **A. D. Franklin**, and A. Afzali-Ardakani, "High purity isolation and quantification of semiconducting carbon nanotubes via column chromatography," *ACS Nano*, vol. 7, pp. 2971-2976, 2013.
33. **A. D. Franklin**, S. Oida, D. B. Farmer, J. T. Smith, S. -J. Han, C. M. Breslin, and L. Gignac, "Stacking graphene channels in parallel for enhanced performance with the same footprint," *IEEE Electron Device Lett.*, vol. 34, pp. 556-558, 2013.
34. **A. D. Franklin**, N. A. Bojarczuk, and M. Copel, "Consistently low subthreshold swing in carbon nanotube transistors using lanthanum oxide," *Appl. Phys. Lett.*, vol. 102, pp. 013108, 2013.
35. **A. D. Franklin**, S. Koswatta, D. B. Farmer, G. S. Tulevski, J. T. Smith, H. Miyazoe, and W. Haensch, "Scalable and fully self-aligned n-type carbon nanotube transistors with gate-all-around," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 4.5.1-4.5.4, 2012.
36. H. Park, A. Afzali, S. -J. Han, G. S. Tulevski, **A. D. Franklin**, J. Tersoff, J. B. Hannon, and W. Haensch, "High-density integration of carbon nanotubes via chemical self-assembly," *Nature Nanotechnol.*, vol. 7, pp. 787-791, 2012.
37. Q. Cao, S. -J. Han, G. S. Tulevski, **A. D. Franklin**, and W. Haensch, "Evaluation of field-effect mobility and contact resistance of transistors that use solution-processed single-walled carbon nanotubes," *ACS Nano*, vol. 6, pp. 6471-6477, 2012.
38. S. -J. Han, D. Reddy, G. D. Carpenter, **A. D. Franklin**, and K. A. Jenkins, "Current saturation in sub- $\mu\text{m}$  graphene transistors with thin gate dielectric: Experiment, simulation, and theory," *ACS Nano*, vol. 6, pp. 5220-5226, 2012.
39. **A. D. Franklin**, M. Luisier, S. -J. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom, and W. Haensch, "Sub-10 nm carbon nanotube transistor," *Nano Lett.*, vol. 12, pp. 758-762, 2012.
40. **A. D. Franklin**, G. S. Tulevski, S. -J. Han, D. Shahrjerdi, Q. Cao, H. -Y. Chen, H. -S. P. Wong, and W. Haensch, "Variability in carbon nanotube transistors: Improving device-to-device consistency," *ACS Nano*, vol. 6, pp. 1109-1115, 2012.

41. **A. D. Franklin**, S. -J. Han, A. A. Bol, and V. Perebeinos, "Double contacts for improved performance of graphene transistors," *IEEE Electron Device Lett.*, vol. 33, pp. 17-19, 2012.
42. **A. D. Franklin**, S. -J. Han, G. S. Tulevski, M. Luisier, C. M. Breslin, L. Gignac, M. S. Lundstrom, and W. Haensch, "Sub-10 nm carbon nanotube transistor," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 23.7.1-23.7.3, 2011.
43. S. -J. Han, A. Valdes-Garcia, A. Bol, **A. D. Franklin**, D. Farmer, K. A. Jenkins, and W. Haensch, "Graphene technology with reversed-T gate and RF passives on 200mm platform," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 2.2.1-2.2.4, 2011.
44. D. Shahrjerdi, **A. D. Franklin**, S. Oida, G. S. Tulevski, S. -J. Han, J. B. Hannon, and W. Haensch, "High device yield carbon nanotube NFETs for high-performance logic applications," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 23.3.1-23.3.4, 2011.
45. S. -J. Han, K. A. Jenkins, A. V. Garcia, **A. D. Franklin**, A. A. Bol, and W. Haensch, "High-frequency graphene voltage amplifier," *Nano Lett.*, vol. 11, pp. 3690-3693, 2011.
46. **A. D. Franklin**, "Replacing silicon with carbon nanotubes—Why it's still worth considering," *EE Web Pulse Magazine*, issue 13, pp. 8-10, 2011.
47. **A. D. Franklin**, S. -J. Han, A. A. Bol, and W. Haensch, "Effects of nanoscale contacts to graphene," *IEEE Electron Device Lett.*, vol. 32, pp. 1035-1037, 2011.
48. S.-J. Han, J. Chang, **A. D. Franklin**, A. A. Bol, R. Loesing, D. Guo, G. S. Tulevski, W. Haensch, and Z. Chen, "Wafer scale fabrication of carbon nanotube FETs with embedded poly-gates," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 9.1.1-9.1.4, 2010.
49. **A. D. Franklin** and Z. Chen, "Length scaling of carbon nanotube transistors," *Nature Nanotechnol.*, vol. 5, pp. 858-862, 2010.
50. **A. D. Franklin**, A. Lin, H. -S. P. Wong, and Z. Chen, "Current scaling in aligned carbon nanotube array transistors with local bottom gating," *IEEE Electron Device Lett.*, vol. 31, pp. 644-646, 2010.
51. R. A. Sayer, S. Kim, **A. D. Franklin**, S. Mohammadi, and T. S. Fisher, "Shot noise thermometry for thermal characterization of templated carbon nanotubes," *IEEE Trans. Components and Packaging Technol.*, vol. 33, pp. 178-183, 2010.
52. T. L. Westover, **A. D. Franklin**, B. A. Cola, T. S. Fisher, and R. G. Reifengerger, "Photo- and thermionic emission from potassium-intercalated carbon nanotube arrays," *J. Vac. Sci. Technol. B*, vol. 28, pp. 423-434, 2010.
53. **A. D. Franklin**, G. Tulevski, J. B. Hannon, Z. Chen, "Can carbon nanotube transistors be scaled without performance degradation?" *IEEE International Electron Device Meeting (IEDM) Technical Digest*, pp. 1-4, 2009.
54. **A. D. Franklin**, R. A. Sayer, T. D. Sands, D. B. Janes, and T. S. Fisher, "Vertical carbon nanotube devices with nanoscale lengths controlled without lithography," *IEEE Trans. Nanotechnol.*, vol. 8, pp. 469-476, 2009. (COVER ARTICLE)
55. **A. D. Franklin**, R. A. Sayer, T. D. Sands, T. S. Fisher, and D. B. Janes, "Toward surround gates on vertical single-walled carbon nanotube devices," *J. Vac. Sci. Technol. B*, vol. 27, pp. 821-826, 2009.
56. J. C. Claussen, **A. D. Franklin**, A. Haque, M. Porterfield, and T. S. Fisher, "Electrochemical biosensor of nanocube-augmented carbon nanotube networks," *ACS Nano*, vol. 3, pp. 37-44, 2009. (COVER ARTICLE)
57. **A. D. Franklin**, J. C. Claussen, T. D. Sands, T. S. Fisher, and D. B. Janes, "Independently addressable fields of porous anodic alumina embedded in SiO<sub>2</sub> on Si," *Appl. Phys. Lett.*, vol. 92, pp. 013122, 2008.
58. R. Voggu, C. S. Rout, **A. D. Franklin**, T. S. Fisher, and C. N. R. Rao, "Extraordinary sensitivity of the electronic structure and properties of single-walled carbon nanotubes to molecular charge-transfer," *J. Phys. Chem. C*, vol. 112, pp. 13053-13056, 2008.
59. J. T. Smith, Q. Hang, **A. D. Franklin**, D. B. Janes, and T. D. Sands, "Highly ordered diamond and hybrid triangle-diamond patterns in porous anodic alumina thin films," *Appl. Phys. Lett.*, vol. 93, pp. 043108, 2008.
60. **A. D. Franklin**, J. T. Smith, T. S. Fisher, T. D. Sands, K.-S. Choi, and D. B. Janes, "Controlled decoration of single-walled carbon nanotubes with Pd nanocubes," *J. Phys. Chem. C*, vol. 111, pp. 13756-13762, 2007.

61. A. D. Franklin, M. R. Maschmann, M. DaSilva, D. B. Janes, T. S. Fisher, and T. D. Sands, "In-place fabrication of nanowire electrode arrays for vertical nanoelectronics on Si substrates," *J. Vac. Sci. Technol. B*, vol. 25, pp. 343-347, 2007. Also, in *Virtual J. Nanoscale Sci. Technol.* 15, Iss. 9, 2007.
62. M. R. Maschmann, A. D. Franklin, T. D. Sands, and T. S. Fisher, "Optimization of porous anodic Al-Fe-Al structures for carbon nanotube synthesis," *Carbon*, vol. 45, pp. 2290-2296, 2007.
63. A. D. Franklin, M. R. Maschmann, A. Scott, D. B. Janes, T. D. Sands, and T. S. Fisher, "Lithography-free *in situ* Pd contacts to templated single-walled carbon nanotubes," *Nano Lett.*, vol. 6, pp. 2712-2717, 2006.
64. M. R. Maschmann, A. D. Franklin, P. B. Amama, D. N. Zakharov, E. A. Stach, T. D. Sands, and T. S. Fisher, "Vertical single- and double-walled carbon nanotubes grown from modified porous anodic alumina templates," *Nanotechnology*, vol. 17, pp. 3925-3929, 2006.

### Conference Proceedings

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1. S. N. Noyce, J. L. Doherty, and A. D. Franklin, "Bias stress stability of carbon nanotube transistors with implications for sensors," *Device Research Conference (DRC) Technical Digest*, (2018).
2. J. A. Cardenas, S. Upshaw, M. J. Catenacci, B. J. Wiley, and A. D. Franklin, "Exploring silver contact morphologies in printed carbon nanotube thin-film transistors," *Device Research Conference (DRC) Technical Digest*, (2018).
3. J. B. Andrews, J. A. Cardenas, J. Mullett, and A. D. Franklin, "Fully printed and flexible carbon nanotube transistors designed for environmental pressure sensing and aimed at smart tire applications," *Proc. IEEE Sensors 2017*, (2017).
4. A. D. Franklin, "Scaling, stacking, and printing: How 1D and 2D nanomaterials still hold promise for a new era of electronics," *VLSI Technology Symposium Technical Digest*, (2017).
5. F. A. McGuire, Y. -C. Lin, B. Rayner, and A. D. Franklin, "MoS2 negative capacitance FETs with CMOS-compatible hafnium zirconium oxide," *Device Research Conference (DRC) Technical Digest*, (2017).
6. Z. Cheng, K. M. Price, and A. D. Franklin, "Edge contacts to multilayer MoS2 using *in situ* Ar ion beam," *Device Research Conference (DRC) Technical Digest*, (2017).
7. K. M. Price and A. D. Franklin, "Integration of 3.4 nm HfO2 into the gate stack of MoS2 and WSe2 top-gate field-effect transistors," *Device Research Conference (DRC) Technical Digest*, (2017).
8. Z. Cheng, J. A. Cardenas, F. McGuire, and A. D. Franklin, "Using Ar ion beam exposure to improve contact resistance in MoS2 FETs," *Device Research Conference (DRC) Technical Digest*, (2016).
9. A. D. Franklin and W. Haensch, "Defining and overcoming the contact resistance challenge in scaled carbon nanotube transistors," *Device Research Conference (DRC) Technical Digest*, (2014).
10. A. D. Franklin, S. Koswatta, D. B. Farmer, G. S. Tulevski, J. T. Smith, H. Miyazoe, and W. Haensch, "Scalable and fully self-aligned n-type carbon nanotube transistors with gate-all-around," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, (2012).
11. A. D. Franklin, S. -J. Han, G. S. Tulevski, M. Luisier, C. M. Breslin, L. Gignac, M. S. Lundstrom, and W. Haensch, "Sub-10 nm carbon nanotube transistor," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, (2011).
12. S. -J. Han, A. Valdes-Garcia, A. Bol, A. D. Franklin, D. Farmer, K. A. Jenkins, and W. Haensch, "Graphene technology with reversed-T gate and RF passives on 200mm platform," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, (2011).
13. D. Shahrjerdi, A. D. Franklin, S. Oida, G. S. Tulevski, S. -J. Han, J. B. Hannon, and W. Haensch, "High device yield carbon nanotube NFETs for high-performance logic applications," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, (2011).
14. S.-J. Han, J. Chang, A. D. Franklin, A. A. Bol, R. Loesing, D. Guo, G. S. Tulevski, W. Haensch, and Z. Chen, "Wafer scale fabrication of carbon nanotube FETs with embedded poly-gates," *IEEE International Electron Device Meeting (IEDM) Technical Digest*, (2010).
15. A. D. Franklin, A. A. Bol, and Z. Chen, "Channel and contact length scaling in carbon nanotube transistors" *Device Research Conference (DRC) Technical Digest*, (2010).
16. A. D. Franklin, G. Tulevski, J. B. Hannon, Z. Chen, "Can carbon nanotube transistors be scaled without performance degradation?" *IEEE International Electron Device Meeting (IEDM) Technical Digest*, (2009).

## Book Chapters

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1. **A. D. Franklin**, "Carbon nanotube electronics," *Emerging Nanoelectronic Devices*, ed. A. Chen, John Wiley & Sons, Ltd, Jan. 2015.
2. **A. D. Franklin**, M. R. Maschmann, and T. S. Fisher, "Integration of vertical carbon nanotube devices," *Encyclopedia of Semiconductor Nanotechnology*, ed. A. Umar, American Scientific Publishers, (in press), 2012.

## Selected Patents

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1. J. B. Andrews, M. A. Brooke, **A. D. Franklin**, "Non-invasive thickness measurement using resonant frequency shift," U.S. Patent 9797703, ISSUED October 24, 2017.
2. J. B. Andrews, M. A. Brooke, **A. D. Franklin**, "Non-invasive thickness measurement using capacitance measurement," PCT Patent: WO 2017/184185 A1, PUBLISHED October 26, 2017.
3. **A. D. Franklin**, S. -J. Han, S. S. Papa Rao, J. T. Smith, "Semiconductor device with ballistic gate length structure," U.S. Patent 9786852 B2, ISSUED October 10, 2017.
4. J. B. Andrews, M. A. Brooke, **A. D. Franklin**, "Non-invasive thickness measurement using resonant frequency shift," PCT Patent: WO 2017/155559 A1, PUBLISHED September 14, 2017.
5. **A. D. Franklin**, S. O. Koswatta, J. T. Smith, "Selective doping of a gate-all-around spacing nanotube transistor," Chinese Patent 104969335 B, ISSUED August 11, 2017.
6. **A. D. Franklin**, H. Miyazoe, S. Oida, J. T. Smith, "Stacked graphene field-effect transistor," U.S. Patent 9711613 B2, ISSUED July 18, 2017.
7. **A. D. Franklin**, J. T. Smith, G. S. Tulevski, "Vertically stacked carbon nanotube transistor formation," Chinese Patent 103824778 B, ISSUED March 1, 2017.
8. **A. D. Franklin**, A. Afzali-Ardakani, G. S. Tulevski, "Self-aligned carbon nanotube transistor including source/drain extensions and top gate," U.S. Patent 9543535 B1, ISSUED January 10, 2017.
9. **A. D. Franklin**, A. Afzali-Ardakani, G. S. Tulevski, "Self-aligned carbon nanotube transistor including source/drain extensions and top gate," U.S. Patent 9543534 B1, ISSUED January 10, 2017.
10. **A. D. Franklin**, H. Miyazoe, S. Oida, J. T. Smith, "Stacked graphene field-effect transistor," U.S. Patent 9508801 B2, ISSUED November 29, 2016.
11. **A. D. Franklin**, M. R. Maschmann, T. S. Fisher, T. D. Sands, "Contact metallization of carbon nanotubes," U.S. Patent 9487877 B2, ISSUED November 8, 2016.
12. S. -J. Han, **A. D. Franklin**, Z. Chen, "Graphene devices with local dual gates," U.S. Patent 9466686 B2, ISSUED October 11, 2016.
13. **A. D. Franklin**, D. B. Farmer, J. T. Smith, "Self-aligned double gate graphene transistor and manufacturing method thereof," Chinese Patent 103855218 B, ISSUED September 28, 2016.
14. **A. D. Franklin**, A. Afzali-Ardakani, G. S. Tulevski, "DNA sequencing using a suspended carbon nanotube," U.S. Patent 9428805 B2, ISSUED August 30, 2016.
15. **A. D. Franklin**, A. Afzali-Ardakani, G. S. Tulevski, "DNA sequencing using a suspended carbon nanotube," U.S. Patent 9371561 B2, ISSUED June 21, 2016.
16. S. -J. Han, **A. D. Franklin**, Z. Chen, "Graphene device having a partial double gate," Chinese Patent 103329244 B, ISSUED June 1, 2016.
17. S. -J. Han, **A. D. Franklin**, Z. Chen, "Graphene devices with local dual gates," U.S. Patent 9306028 B2, ISSUED April 5, 2016.
18. **A. D. Franklin**, S. -J. Han, S. S. Papa Rao, J. T. Smith, "Semiconductor device with ballistic gate length structure," U.S. Patent 9246112 B2, ISSUED January 26, 2016.
19. **A. D. Franklin**, G. S. Tulevski, J. T. Smith, "Device for electrical characterization of molecules using CNT-nanoparticle-molecule-nanoparticle-CNT structure," U.S. Patent 9123454 B2, ISSUED September 1, 2015.
20. Y. Astier, J. Bai, R. L. Bruce, **A. D. Franklin**, J. T. Smith, "Nanoporous structures by reactive ion etching," U.S. Patent 9117652 B2, ISSUED August 25, 2015.

21. **A. D. Franklin**, J. T. Smith, G. S. Tulevski, "Transistors from vertical stacking of carbon nanotube thin films," U.S. Patent 9105702 B2, ISSUED August 11, 2015.
22. **A. D. Franklin**, J. T. Smith, G. S. Tulevski, "Transistors from vertical stacking of carbon nanotube thin films," U.S. Patent 9099542 B2, ISSUED August 4, 2015.
23. S. -J. Han, **A. D. Franklin**, Z. Chen, "Graphene devices with local dual gates," U.S. Patent 9082856 B2, ISSUED July 14, 2015.
24. S. -J. Han, **A. D. Franklin**, Z. Chen, "Graphene devices with local dual gates," U.S. Patent 9076873 B2, ISSUED July 7, 2015.
25. **A. D. Franklin**, S. -J. Han, A. A. Bol, "Semiconductor device including graphene layer and method of making the semiconductor device," U.S. Patent 9064842 B2, ISSUED June 23, 2015.
26. J. T. Smith, **A. D. Franklin**, G. S. Tulevski, D. B. Farmer, "Carbon nanotube devices with unzipped low-resistance contacts," U.S. Patent 9040364 B2, ISSUED May 26, 2015.
27. J. T. Smith, **A. D. Franklin**, G. S. Tulevski, D. B. Farmer, "Carbon nanotube devices with unzipped low-resistance contacts," U.S. Patent 9029841 B2, ISSUED May 12, 2015.
28. **A. D. Franklin**, S. O. Koswatta, J. T. Smith, "Gate-all-around carbon nanotube transistor with selectively-doped spacers," U.S. Patent 9000499 B2, ISSUED April 7, 2015.
29. **A. D. Franklin**, G. S. Tulevski, J. T. Smith, "Device for electrical characterization of molecules using CNT-nanoparticle-molecule-nanoparticle-CNT structure," U.S. Patent 8968582 B2, ISSUED March 3, 2015.
30. **A. D. Franklin**, J. T. Smith, D. B. Farmer, S. Oida, "Vertical stacking of graphene in a field-effect transistor," U.S. Patent 8932919 B2, ISSUED January 13, 2015.
31. **A. D. Franklin**, S. -J. Han, Z. Chen, "Vertical stacking of carbon nanotube arrays for current enhancement and control," U.S. Patent 8890116 B2, ISSUED November 18, 2014.
32. **A. D. Franklin**, T. D. Sands, T. S. Fisher, D. B. Janes, "Field effect transistor fabrication from carbon nanotubes," U.S. Patent 8872154, ISSUED October 28, 2014.
33. **A. D. Franklin**, J. T. Smith, D. B. Farmer, S. Oida, "Vertical stacking of graphene in a field-effect transistor," U.S. Patent 8809837 B2, ISSUED August 19, 2014.
34. **A. D. Franklin**, D. B. Farmer, J. T. Smith, "Self-aligned double-gate graphene transistors," U.S. Patent 8803132 B2, ISSUED August 12, 2014.
35. **A. D. Franklin**, D. B. Farmer, J. T. Smith, "Self-aligned double-gate graphene transistors," U.S. Patent 8796096 B2, ISSUED August 5, 2014.
36. Z. Chen, **A. D. Franklin**, S. -J. Han, J. B. Hannon, K. L. Saenger, G. S. Tulevski, "Graphene or carbon nanotube devices with localized bottom gates and gate dielectric," U.S. Patent 8785911 B2, ISSUED July 22, 2014.
37. D. B. Farmer, **A. D. Franklin**, S. -J. Han, G. S. Tulevski, "Self-aligned carbon nanostructure field effect transistors using selective dielectric deposition," U.S. Patent 8786018 B2, ISSUED July 22, 2014.
38. D. B. Farmer, **A. D. Franklin**, S. -J. Han, G. S. Tulevski, "Self-aligned carbon nanostructure field effect transistors using selective dielectric deposition," U.S. Patent 8785262 B2, ISSUED July 22, 2014.
39. J. T. Smith, **A. D. Franklin**, C. D. Dimitrakopoulos, "Transport conduits for contacts to graphene," U.S. Patent 8772098 B2, ISSUED July 8, 2014.
40. D. B. Farmer, **A. D. Franklin**, S. -J. Han, G. S. Tulevski, "Area-efficient capacitor using carbon nanotubes," U.S. Patent 8765547 B2, ISSUED July 1, 2014.
41. D. B. Farmer, **A. D. Franklin**, S. -J. Han, G. S. Tulevski, "Area-efficient capacitor using carbon nanotubes," U.S. Patent 8766345 B2, ISSUED July 1, 2014.
42. **A. D. Franklin**, J. T. Smith, Q. Cao, "Double contacts for carbon nanotube thin film devices," U.S. Patent 8754393 B2, ISSUED June 17, 2014.
43. **A. D. Franklin**, J. T. Smith, S. -J. Han, P. M. Solomon, "Contacts-first self-aligned carbon nanotube transistor with gate-all-around," U.S. Patent 8741756 B2, ISSUED June 3, 2014.

44. **A. D. Franklin**, J. T. Smith, Q. Cao, "Double contacts for carbon nanotube thin film devices," U.S. Patent 8741751 B2, ISSUED June 3, 2014.
45. J. C. Claussen, **A. D. Franklin**, T. S. Fisher, D. M. Porterfield, "Electrochemical biosensor," U.S. Patent 8715981 B2, ISSUED May 6, 2014.
46. J. T. Smith, **A. D. Franklin**, C. D. Dimitrakopoulos, "Sub-10nm graphene nanoribbon lattices," U.S. Patent 8685844 B2, ISSUED April 1, 2014.
47. **A. D. Franklin**, J. T. Smith, S. -J. Han, P. M. Solomon, "Contacts-first self-aligned carbon nanotube transistor with gate-all-around," U.S. Patent 8674412 B2, ISSUED March 18, 2014.
48. J. T. Smith, **A. D. Franklin**, C. D. Dimitrakopoulos, "Transport conduits for contacts to graphene," U.S. Patent 8637850, ISSUED January 28, 2014.
49. **A. D. Franklin**, S. O. Koswatta, J. T. Smith, "Gate-all-around carbon nanotube transistor with selectively-doped spacers," U.S. Patent 8609481 B1, ISSUED December 17, 2013.
50. **A. D. Franklin**, J. B. Hannon, G. Tulevski, Z. Chen, "Local bottom gates for graphene and carbon nanotube devices," U.S. Patent 8587065 B2, ISSUED November 19, 2013.
51. **A. D. Franklin**, S. -J. Han, Z. Chen, "Vertical stacking of carbon nanotube arrays for current enhancement and control," U.S. Patent 8288759 B2, ISSUED October 16, 2012.
52. **A. D. Franklin**, J. B. Hannon, G. Tulevski, Z. Chen, "Local bottom gates for graphene and carbon nanotube devices," U.S. Patent 8124463 B2, ISSUED February 28, 2012.

### Invited Talks

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1. [upcoming] Material Research Society (MRS) Fall Meeting, "TBD," Boston, MA, Nov. 2018.
2. [upcoming] International Mechanical Engineering Congress & Exposition (IMECE), "Harnessing the Versatility of Carbon Nanotubes as Printed Thin Films," Pittsburgh, PA, Nov. 2018.
3. [upcoming] International Workshop on Nano/Micro 2D-3D Fabrication, Manufacturing of Electronic-Biomedical Devices & Applications (IWNEBD), "Ultrasensitive Carbon Nanotubes and Low-Cost Printing for Point-of-Care Biomedical Diagnostics," IIT-Mandi, Mandi, India, Nov. 2018.
4. 2D Materials Summer School, "2D material devices," Univ. Minnesota, Minneapolis, MN, June 2018.
5. 62<sup>nd</sup> International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN), "Scaling, stacking, and printing: How nanomaterials still hold promise for electronics," Rio Grande, Puerto Rico, May 2018.
6. Electrochemical Society (ECS) Meeting, "Improving conducting and insulating interfaces to 2D materials," Seattle, WA, May 2018.
7. [Keynote] Sixteenth IEEE Workshop on Microelectronics and Electron Devices (WMED), "Nanomaterials for a new era of electronic devices: Extending and transforming the trend," Boise, ID, Apr. 2018.
8. Material Research Society (MRS) Spring Meeting, "Harnessing the versatility of carbon nanotubes for printed electronics," Phoenix, AZ, Apr. 2018.
9. Palo Alto Research Center (PARC), "Harnessing the versatility of carbon nanotubes for printed electronics," PARC, Palo Alto, CA, Dec. 2017.
10. ORaCEL Seminar, "Scaling, stacking, and printing: How nanomaterials still hold promise for a new era of electronics," NC State, Raleigh, NC, Sept. 2017.
11. XXVI International Materials Research Congress 2017, "Printing of biologicals and nanomaterials for point-of-care assays," Cancun, Mexico, Aug. 2017.
12. International Workshop on 2D Atomic Sheets, "Harnessing the Unique Usefulness of 2D Materials Through Scaling, Stacking, and Printing," College Park, MD, July 2017.
13. 2017 Symposium on VLSI Technology, "Scaling, stacking, and printing: How 1D and 2D nanomaterials still hold promise for a new era of electronics," Kyoto, Japan, June 2017.



14. Illumina, "Scaling, printing, and sensing: A new era for electronics made possible using nanomaterials," San Diego, CA, Jan. 2017.
15. Brigham Young University, "Scaling, printing, and sensing: A new era for electronics made possible using nanomaterials," Provo, UT, Oct. 2016.
16. IBM T. J. Watson Research Center, "Scaling, printing, and sensing: A new era for electronics made possible using nanomaterials," Yorktown Heights, NY, July 2016.
17. International Symposium on Devices and Applications of Two-Dimensional Materials, "Stacking, damaging, and etching: Optimizing performance in 2D electronic devices," Fudan University, Shanghai, China, July 2016.
18. Emerging Technologies CMOS 2016 Conference, "Promises and challenges of nanomaterial in transistors: From high-performance to thin-film applications," Montreal, Quebec, Canada, May 2016.
19. TechConnect World 2016 - Nanotech, Microtech, Biotech, Cleantech, "Promises, problems, and practicalities of nanomaterials in transistors," National Harbor, MD, May 2016.
20. Phi Theta Kappa Honors Society General Meeting, "How the world works: Global perspectives," Mesa Community College, Mesa, AZ, Mar. 2016.
21. BYU Management Society - Phoenix-East Chapter, "The hidden truth behind our explosive technological revolution," Arizona State University, Tempe, AZ, Mar. 2016.
22. University of Minnesota, "Promises, problems, and practicalities for nanomaterials in transistors," Minneapolis, MN, Mar. 2016.
23. University of Notre Dame, "Promises, problems, and practicalities for nanomaterials in transistors," South Bend, IN, Jan. 2016.
24. MRS-ASM-AVS Joint Symposium, "Nanomaterials in Electronics," NC State, Raleigh, NC, Nov. 2015.
25. [Keynote] 41<sup>st</sup> Micro and Nano Engineering (MNE) conference, "Promises, problems, and practicalities of nanomaterial electronics," The Hague, Netherlands, Sept. 2015.
26. Eindhoven University of Technology, "What role will nanomaterials play in electronics?" Eindhoven, Netherlands, Sept. 2015.
27. Illumina, "The pillars of nanomaterial-enabled devices: Purity, placement, and performance," San Diego, CA, Aug. 2015.
28. North Carolina State University, "What role will nanomaterials play in electronics?" Raleigh, NC, June 2015.
29. Army Research Laboratory (ARL), "Nanomaterials in the Next Switch?" Adelphi, MD, Apr. 2015.
30. University of North Carolina at Chapel Hill, "What role will nanomaterials play in electronics?" Chapel Hill, NC, Apr. 2015.
31. Government Microcircuit Applications & Critical Technology Conference (GOMAC Tech), "Nanomaterials in the next-switch?" St. Louis, MO, Mar. 2015.
32. American Chemical Society (ACS) Meeting, "How will carbon nanotubes impact the next generation of electronics?" Denver, CO, Mar. 2015.
33. Gordon Research Conference—Nanostructure Fabrication, "Prospects for bottom-up 1D and 2D nanoelectronics in high-performance computing," Biddeford, ME, Jul. 2014.
34. TechConnect World 2014 - Nanotech, Microtech, Biotech, Cleantech, "Prospects and challenges for carbon nanotube transistors in high performance nanoelectronics beyond 2020," National Harbor, MD, June 2014.
35. Device Research Conference (DRC) - Rump Session, "What are 2D devices and materials good for?" Santa Barbara, CA, Jun. 2014.
36. 1<sup>st</sup> International Workshop on Data-Abundant System Technology, "Latest advancements toward a carbon nanotube transistor technology," Stanford University, Palo Alto, CA, Apr. 2014.
37. Columbia University, "Next generation transistors: Where do carbon nanotubes fit in?," New York, NY, Mar. 2014.

38. Duke University, "Next generation transistors: Where do carbon nanotubes fit in?," Durham, NC, Feb. 2014.
39. International Semiconductor Device Research Symposium (ISDRS), "Latest developments toward a carbon nanotube transistor technology," Bethesda, MD, Dec. 2013.
40. Lithography Workshop, "Patterning needs and obstacles for a sub-10 nm carbon nanotube transistor technology," La Quinta, CA, Nov. 2013.
41. International Conference on Solid State Devices and Materials (SSDM), "Wrapping carbon nanotubes in a gate-all-around geometry," Fukuoka, Japan, Sept. 2013.
42. National Institute of Advanced Industrial Science and Technology (AIST), "The road ahead for transistors: Where do carbon nanotubes fit in?," Tsukuba, Japan, Sept. 2013.
43. Symposium on Recent Advances in Carbon-Based Nanoelectronics, "Scaling carbon nanotube transistors for a sub-10 nm digital technology," Peking University, Beijing, China, Jul. 2013.
44. Purdue University, "The road ahead for carbon nanotube transistors," West Lafayette, IN, Jun. 2013.
45. Arizona State University, "The road ahead for transistors," Tempe, AZ, Jun. 2013.
46. Material Research Society (MRS) Spring Meeting, "Nanoscale contacts to carbon nanomaterials," San Francisco, CA, Apr. 2013.
47. Stanford University, "Carbon nanotube transistor technology—Are we there yet?!", Palo Alto, CA, Apr. 2013.
48. University of California-Berkeley, "Digital technology from carbon nanotube transistors," Berkeley, CA, Apr. 2013.
49. CNTs for Digital Electronics Workshop, "Scaling and variability," NIST, Gaithersburg, MD, Sept. 2012.
50. Gordon Research Conference - Nanostructure Fabrication, "Carbon Nanotubes for a New Generation of Transistors," University of New England, Biddeford, ME, Jul. 2012.
51. Georgia Institute of Technology, "Carbon Nanotubes—Why They're Still Worth Pursuing for Next-Generation Transistors", Atlanta, GA, Mar. 2012.
52. IBM Materials Research Community, "Promises and Challenges for Achieving a Digital Technology with Carbon Nanotube Transistors," Yorktown Heights, NY, Mar. 2012.
53. NYS Meeting of the American Physical Society, "Carbon nanotubes: Can they really replace silicon?" University of Albany, NY, Apr. 2011.
54. Lester Eastman Conference on High Performance Devices, "Interfacing with carbon nanomaterials—difficulties in accessing the intrinsic properties," Rensselaer Polytechnic Institute, NY, Aug. 2010.
55. University of Notre Dame, "Carbon nanotube transistors: The future?," Notre Dame, IN, Mar. 2009.
56. Arizona State University, "Toward manufacturable vertical carbon nanotube nanoelectronic devices," Tempe, AZ, Nov. 2008.
57. IBM T. J. Watson Research Center, "Templated vertical carbon nanotubes for nanoelectronics," Yorktown Heights, NY, Sept. 2008.

### Grants and Sponsored Research Projects

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1. co-PIs: A. D. Franklin, A. Chilkoti, J. Rogers, "Point-of-care testing to improve monitoring of LVAD patients," *NIH R21, NHLBI*  
\$417,260: Jun. 2018 - May 2020
2. PI: A. D. Franklin, "Exploration of materials and geometries for understanding printed thickness sensors," *Tyrata, Inc.*  
\$46,000: Jan. 2018 - Jul. 2019
3. co-PIs: A. D. Franklin, A. Chilkoti, "A Point-of-Injury Screening Assay for Tactical Damage Control Resuscitation," *CDMRP: Defense Medical Research and Development, JPC-6 Combat Casualty Care Research Program*  
\$1,500,000: Sept. 2017 - Sept. 2020

4. **co-PIs: A. D. Franklin**, D. Mitzi, "Development of Low-Electron Affinity Buffer Layers for High Performance Earth-Abundant Solar Cells," *Duke Energy Research Seed Funding* \$39,864: Jul. 2017 - Jun. 2018
5. **PI: A. D. Franklin**, "Understanding and Accessing the Ultra-sensitivity of Carbon Nanotubes," *Duke School of Medicine (SOM) Facility Voucher Program* \$9,000: Jan. 2017 - Dec. 2017
6. **PI: A. D. Franklin**, "1.2.2 Nanoelectronics and nanosensors for Army applications: Exploring the vertical to plane electronic properties of layered two-dimensional materials," *Army Research Lab (ARL)* \$35,000: Sept. 2016 - Aug. 2017
7. **PI: A. D. Franklin**, "EAGER: Exploring the Negative Capacitance Effect from Hf-based Ferroelectrics and 2D Nanomaterials for Low-Voltage Transistors," *National Science Foundation (NSF)* \$150,000: Oct. 2016 - Sept. 2018
8. **PI: A. D. Franklin**, "Arrays of nanowire transistors: Fabrication and device performance," *Illumina, Inc* \$450,000: Apr. 2016 - Apr. 2019
9. **PI: A. D. Franklin**, "Engineering Atomic Layer Deposited Contact Interfaces to Low-Dimensional Nanomaterials for Improved Scaled Transistor Performance," *National Science Foundation (NSF)* \$358,086: June 2015 - May 2018
10. **PI: A. D. Franklin; co-PI: M. Brooke**, "Nanomaterial-Enabled Printed Electronics for Advanced Tire Monitoring System," *Fetch Automotive Design Group, LLC* \$380,998: July 2015 - Apr. 2017
11. **PI: A. D. Franklin; co-PIs: M. Therien, J. Liu**, "Printing Electronic Circuits Using Nanomaterial Inks," *Duke Pratt Seed Fund* \$37,600: Nov. 2014 - Nov. 2015

## Academic and Professional Service

### Academic Roles

**Director of Graduate Studies:** *Duke, ECE Department* (Sept. 2017 - present)

### Journals & Proposals

**Editorial Advisory Board Member:** *ACS Applied Nano Materials* (2017 - present)

**Journal Reviewer:** *Science, Nature, Nature Nanotechnol., Nature Comm., Nano Lett., ACS Nano, ACS Appl. Mater. Interfaces, Sci. Adv., Sci. Rep., Appl. Phys. Lett., Adv. Mater., Adv. Func. Mater., Adv. Electronic Mater., Adv. Mater. Interfaces, PLOS One, IEEE Trans. Nanotechnol., IEEE Electron Device Lett., IEEE Trans. Electron Devices, Nanotechnology, Thin Solid Films, J. Phys. D: Appl. Phys., MRS Proceedings, New J. Phys., J. Phys. Chem., J. Electronic Mater., Surface Rev. Lett., Mater. Chem. Phys., Physica B: Condensed Matter, Nanoscale Res. Lett., MRS Comm., J. Computational Electronics, Appl. Phys. A, Semicond. Sci. Technol., Nano Res.*

**Grant/Proposal Reviewer:** *National Science Foundation* (since 2011)

### Conference Organization

**General Chair:** *76<sup>th</sup> Device Research Conference - DRC* (2018)

**Technical Program Chair:** *75<sup>th</sup> Device Research Conference - DRC* (2017)

**Technical Program Vice-Chair:** *74<sup>th</sup> Device Research Conference - DRC* (2016)

**Subcommittee Chair:** *International Electron Device Meeting (IEDM), Nano Device Technology* (2017)

**Technical Program Committee Member:** *International Electron Device Meeting - IEDM* (2014 - 2017), *Device Research Conference - DRC* (2012 - present), *International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication - EIPBN* (2014 - 2016), *IEEE Photonics Society Summer Topical Meeting* (2015), *Gordon Research Conference - Nanostructure Fabrication* (2014)

**Session/Symposium Organizer:** *TechConnect Nanoelectronics Section* (June 2015), *Materials Research Society - MRS* (Fall 2014, Fall 2012), *Applied Physics Society Meeting - APS* (March 2013), *IEEE International Conference on Nanotechnology - IEEE Nano* (Aug. 2013)

**Short Course Organizer:** *Device Research Conference - DRC* (2013, "2D Materials Beyond Graphene")

**Workshop Co-organizer:** *Carbon Nanotubes for Digital Electronics Workshop @ NIST* (2012)

**IBM Physical Science Department Seminar Chair**

2011 - 2013

Academic Committees

**(Duke-wide) Misconduct in Research Committee:** *Appointed member* (Sept. 2017 – Aug. 2020)

**(Duke-wide) Academic Council:** *Elected member* (Aug. 2015 – Aug. 2017)

**(Pratt-wide) Engineering Faculty Council:** *Elected member* (Aug. 2015 – Aug. 2017)

**ECE Department:** *Graduate Studies Committee GSC* (Sept. 2017 – present), *Undergraduate Studies Committee UGSC* (Sept. 2016 – Aug. 2017), *TOP ECE Faculty Recruitment Committee* (Spring 2017 – present), *ECE Diversity Committee* (Spring 2017 – present), *ECE Staff Assistant Hiring Committee* (Apr. 2015)

**Chemistry Department:** *Regular Rank Non Tenure Track Faculty Development* (2017-2018), *Research Propositional Examination Committee* (Fall 2015), *Research Faculty Committee* (2015 – 2016)

**Miscellaneous:** *Shared Materials Instrumentation Facility (SMIF) Advisory Committee* (Aug. 2015 – present), *Pratt Dean Search Engineering Faculty Council Committee* (Nov. – Dec. 2015), *Dean's Award for Excellence in Mentoring Selection Committee* (Dec. 2015)

Examination Committees

**Final Defense:** *Xinyu Liu* (July 2017), *David Miller* (Nov. 2016), *Liji Chen* (June 2016), *Erich Radauscher* (Apr. 2016)

**Preliminary Exams:** *Xin Song* (Nov. 2017), *Zhihui Cheng* (Sept. 2017), *Jimmy Thostenson* (July 2017), *Wiley Dunlap-Shohl* (June 2017), *Felicia McGuire* (May 2017), *Callie Woods* (Apr. 2017), *Mutya Cruz* (Apr. 2017), *Xinyu Liu* (Sept. 2016), *Ugonna Ohiri* (June 2016), *Daniel Joh* (May 2016), *Christopher Reyes* (Apr. 2016), *George Bullard* (Apr. 2016), *Qiwei Han* (Apr. 2015), *Lianjun Ellie Zheng* (Apr. 2015), *Matthew Catenacci* (Apr. 2015), *Erich Radauscher* (Mar. 2015)

**Qualifying Exams:** *Tomas Barraza* (Nov. 2017), *Haibei Zhu* (Nov. 2017), *Evan Stump* (Nov. 2017), *Xander Deputy* (Nov. 2017), *Jorge Cardenas* (Oct. 2017), *Shruti Preetam* (Oct. 2017), *Spencer Ferguson* (Oct. 2017), *Wade Wilson* (May 2017), *Fan Wang* (Apr. 2017), *Raul Vyas* (Dec. 2016), *Steven Noyce* (Dec. 2016), *Philip Herr* (Dec. 2016), *Xin Song* (Dec. 2016), *Tasso von Windheim* (Nov. 2016), *Zhongxi Li* (Nov. 2016), *Yuh-Chen Lin* (Nov. 2016), *Katherine Price* (June 2016), *Wiley Dunlap-Shohl* (June 2016), *Jimmy Thostenson* (Apr. 2016), *Zhihui Cheng* (Feb. 2016), *Laura Pulido* (Oct. 2015), *Callie Woods* (Sept. 2015), *Felicia McGuire* (Apr. 2015)

Prior to Duke

**Corporate Liaison from IBM:** *SRC-GRC Task at Georgia Tech* (2010 – 2014), *Nanoelectronics Research Initiative (NRI) funded centers* (2010 – 2013)

**Purdue University ECE Graduate Committee Member** 2008

**Birck Nanotechnology Center Student Advisory Councilmember, Purdue University** 2006 – 2008

**Graduate Student Mentor to Undergraduate Research Fellows, Purdue University** 2006 – 2007

Research and Professional Experience

**Tyrata, Inc., Durham, NC** 2017 – Present

*Co-Founder & Chief Technology Officer (CTO)*

- Start-up company based on technology from my Duke research lab for printed tire tread wear sensors.
- Helped secure series A funding of \$4.5M to start company.
- Lead intellectual property generation and protection efforts.
- Maintain technology roadmap and competitive technology analysis.

**Duke University, Durham, NC**

*Associate Professor, Department of Electrical and Computer Engineering & Department of Chemistry* 2014 – Present

- Direct research program on nanoelectronics and printed electronic devices for diverse applications.
- Support the teaching mission of the university in both undergraduate and graduate education.
- Serve the academic community through committee work, both research and administrative in nature.
- Establish and maintain international recognition for students/research coming out of the lab.

**IBM, T. J. Watson Research Center, Yorktown Heights, NY**

*Research Staff Member* 2008 – 2014

- Investigated low-dimensional materials for electronics applications.
- Developed integration processes for carbon nanotubes and graphene into nanoelectronic devices.
- Studied and improved scaling behavior in carbon nanotube and graphene devices.
- Explored application of carbon nanotubes to supercapacitor electrodes.
- Studied thin-film transistors from carbon nanotubes and graphene for flexible electronics applications.
- Implemented carbon nanotubes and/or graphene for electrodes in photovoltaic cells.

**Purdue University, Birck Nanotechnology Center, School of Electrical and Computer Engineering**, West Lafayette, IN  
*NSF Fellow, PhD Student* 2005 – 2008

- Developed process for nanowire growth by penetrating alumina barrier in porous anodic alumina (PAA).
- Optimized electrodeposition process to achieve controlled formation of Pd nanocubes decorating CNTs for application in biosensors.
- Conducted extensive optimization studies on CNT synthesis using plasma-enhanced CVD.
- Designed and implemented technique for obtaining long-range ordered thin-film PAA.
- Developed process for embedding PAA in customizable patterns within SiO<sub>2</sub>.
- Fabricated and characterized the first completely vertical two-terminal CNT devices.
- Established surround gates on vertical CNT channels.
- Developed process for straightforward control of CNT channel length for vertical nanoelectronics.

**Intel Corporation**, Chandler, AZ 2004 – 2005  
*Component Design Engineer*

- Designed and validated various units for the Intel chipset projects.
- Implemented and enhanced skills in logic design, debugging, and project management.

**Institute for Nanoelectronics and Computing, Purdue University**, West Lafayette, IN 2004  
*NASA Summer Undergraduate Research Intern*

- Studied effects of pre-growth catalyst annealing on CNT synthesis in plasma-enhanced CVD.
- Contributed to the design/characterization of modified PAA for synthesizing vertical CNT channels.

**Honeywell**, Phoenix, AZ 2003 – 2004  
*Electrical Engineer Intern (Automated Flight Controls Systems)*

- Performed manual computer tests on various mixed signal designs.
- Sponsored by Corporate Leaders Program, which provided interaction with industry leaders and enhancement of communication and presentation skills through monthly activities.

**Arizona State University, Department of Electrical Engineering**, Tempe, AZ 2003 – 2004  
*Undergraduate Researcher*

- Performed electrical characterization of solid-state ionic memory devices.

## Teaching Experience

**Duke University**, Durham, NC 2014 – present  
*Associate Professor, Department of Electrical & Computer Engineering and Department of Chemistry*

- *ECE 230L* – Fall 2018. Revised & taught undergraduate core course on semiconductor physics & devices.
- *ECE 512* – Spring 2018. Updated and taught graduate-level course on nanoelectronic devices.
- *ECE 230L* – Fall 2017. Taught undergraduate core course on microelectronic devices & circuits.
- *ECE 230L* – Spring 2017. Taught undergraduate core course on microelectronic devices & circuits.
- *ECE/NANOSCI 511* – Spring 2017. Updated content for, developed, and taught graduate-level course on foundations of nanoscale science & technology.
- *ECE 230L* – Fall 2016. Taught undergraduate core course on microelectronic devices & circuits.
- *ECE 590.05* – Spring 2016. Updated and taught graduate-level course on nanoelectronic devices.
- *ECE 230L* – Fall 2015. Taught undergraduate core course on microelectronic devices & circuits.
- *CHEM 548* – Spring 2015. Developed and taught graduate-level course on solid-state materials/chemistry.
- *ECE 590.08* – Fall 2014. Developed and taught graduate-level course on nanoelectronic devices.

**Columbia University**, New York, NY 2013 – 2014  
*Adjunct Assistant Professor, Department of Electrical Engineering*

- Developed and taught graduate-level courses on emerging and low-dimensional nanoelectronic devices.

**Ivy Tech Community College**, Lafayette, IN 2007 – 2008  
*Adjunct Faculty*

- Taught undergraduate math courses, including all lecturing and grading.
- Received highest ratings in department from student reviews.

## Community Service

**IBM Mentor to High School Students** 2011 – 2014  
 Pathways in Technology Early College High School (P-TECH)

- One-on-one mentoring of P-TECH students in STEM disciplines.

**National Engineers Week Volunteer** 2005, 2011 – present  
 Intel Corporation, IBM, Duke

- Judge local and national high school science fair projects.

- Visit high school science classes to motivate students to pursue careers in science and engineering.

**High School Seminary Teacher**

2001 - 2007

- Daily taught two high school seminary classes of 30+ students for four years.

**Global Tech Leaders Symposium Delegate**

2004

Corporate Leaders Program, Arizona State University

- Worked in diverse teams to provide technological service to communities in Singapore and Tokyo.

**Boy Scouts of America Explorer Post Leader**

2001 - 2003

- Led group of 15 boys through high-adventure activities and character-building merit badge classes.

**Full-time Church Missionary**

1998 - 2000