Unanticipated Polarity Shift in Edge-Contacted Tungsten-Based 2D Transition Metal Dichalcogenide Transistors

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***Abstract*— Creating metal edge contacts in transition metal dichalcogenide (TMD) transistors is a promising path to advance transistor miniaturization for future technology nodes. Current experimental demonstrations nearly exclusively focus on MoS_2 as the channel material. Here, we create edge-contacted WSe_2 and WS_2 transistors using a convergent Ar^+ ion beam source integrated within an e-beam evaporator chamber for *in-situ* processing. An unanticipated polarity shift was observed compared to top-contact behavior for Ti-WS_2 devices, which displayed p-type conduction. Meanwhile, three distinct metal contact materials yielded comparable p-branch-dominant performance on WSe_2. Transmission electron microscope (TEM) imaging with energy dispersive spectroscopy (EDS) analysis indicated the existence of a residual layer of W (and chalcogen atoms to a lesser extent) beneath the metal contacts, even though the substrate was over-etched. The images presented a physically pure edge interface. This intriguing etching effect could carry significant implications for the design of tungsten-based, edge-contacted TMD transistors.**

***Index Terms*— Edge contacts, transition metal dichalcogenide (TMD), field-effect transistor (FET), carrier injection, ion beam.**

I. Introduction

THE experimental demonstration of air-stable monolayers of graphene in 2004 generated overwhelming interest in 2D materials [1]. One subfamily of the 2D crystals, the transition metal dichalcogenides (TMD), emerged as a strong candidate for atomically thin-body field-effect transistors (FETs) [2]. Despite showing excellent performance, 2D FETs as they stand cannot compete with state-of-the-art silicon FinFETs. One of the main disadvantages is the high contact resistance (R_C) that forms at the interface between the metal contact and the TMD surface [3]. Injected carriers in 2D FETs must tunnel through a physical vdW gap [4] in addition to a substantial Schottky barrier that often arises from strong Fermi level pinning-like behavior [5], [6].

Researchers have reported several techniques to address the contact resistance challenge. The suggested solutions include using semi-metallic metal contact [7], [8], adding an interlayer [8], post-process annealing [9], doping [10], [11], surface phase engineering [12], and ion bombardment [13], [14]. Another, less-investigated path towards improving metal-2D contacts involves changing the contact configuration from a top contact to an edge contact. While TMD surfaces are generally inert, their sides are reactive, which should translate to covalent bonds forming at the metal-TMD interface and a vanishing vdW tunneling gap [15]. More importantly, edge contacts offer maximum device scalability [16] and 3D integration compatibility.

There is an expansive library of semiconducting TMDs that have not been examined yet for edge-contacted transistors [17]; in fact, experimental reports to date are almost exclusively focused on MoS_2 [16], [18]–[23] with the exception of the work by Chu *et al.* [24] and the WS_2 300 mm pilot line integration work at imec, which reported an unanticipated and unexplained p-type polarity shift [25], [26]. In this study, we report edge-contacted transistors made from the less-explored WSe_2 and WS_2 using a facile fabrication strategy and explore the underlying cause of the unanticipated polarity shift. The fabrication setup yields clean edge contacts by utilizing an *in-situ* ion beam source embedded in a high-vacuum evaporation chamber [16].

II. Device Fabrication

The major processing steps in creating the edge-contacted transistors in this study are shown in Fig. 1(a). WSe_2 and WS_2 films were grown directly using chemical vapor deposition (CVD) on Si p^{++} substrates with 300 nm SiO_2 at 850 °C. Subsequently, the chips were coated with polymethyl methacrylate (PMMA) resist and alignment marks were patterned using electron beam lithography (EBL). 20 nm Ti/20 nm Au were deposited to form the alignments marks. After that, suitable TMD regions were located to pattern as the transistor channels. The as-grown film covers the entire

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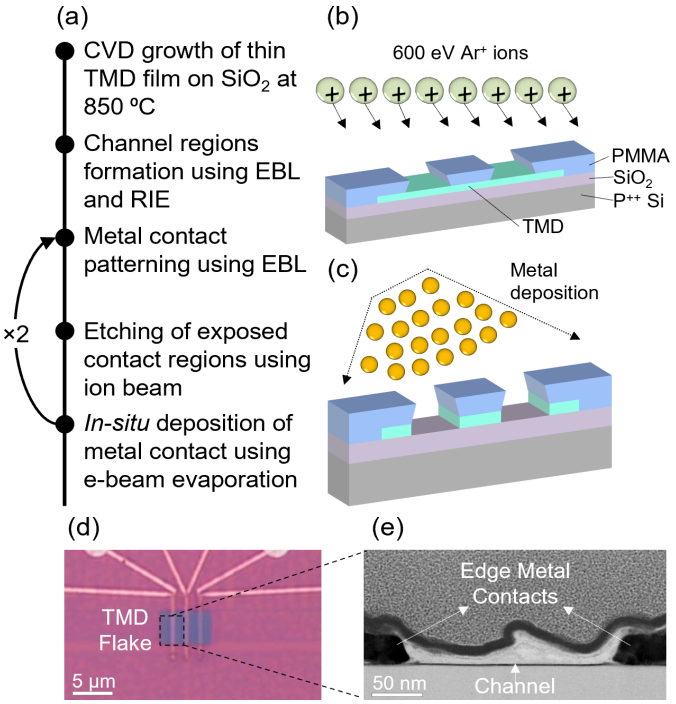

Fig. 1. Fabrication of edge contacts on WS_2 and WSe_2 using *in-situ* Ar^+ ion beam. (a) Major processing steps (steps 3-5 are repeated two more times to yield three distinct contact materials on the same channel). (b) Schematic of *in-situ* ion beam etching step to expose TMD edge. (c) Schematic of e-beam evaporation step immediately after ion beam irradiation to create source and drain contacts. (d) Optical image of a finished device set. (e) Cross-sectional TEM image of one device within a device set. RIE: reactive ion etching.

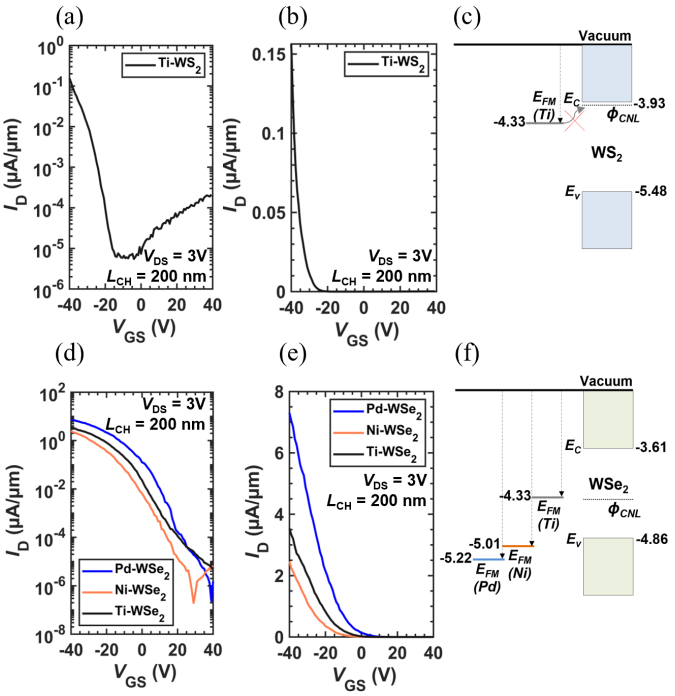

Fig. 2. Characteristics of the edge-contacted WS_2 and WSe_2 FETs. (a-b) Subthreshold and transfer I-V characteristics of trilayer edge-contacted Ti-WS_2 device showing unanticipated p-type conduction. (c) Conceptual energy band alignment based on clean metal work functions of the Ti-WS_2 system (energies are in eV). (d-e) Subthreshold and transfer I-V characteristics of three distinct edge-contact metals on the same bilayer WSe_2 channel exhibiting similar performance. (f) Conceptual energy band alignment based on clean metal work functions of the metal-WSe_2 systems. All measurements were done at room temperature. ϕ_{CNL}: charge neutrality level. E_{FM}: metal Fermi level.

substrate, so EBL patterning was used to form resist bars over the channels followed by a reactive ion etch (RIE) to cleanly remove the TMD from essentially everywhere but the channel regions. For the RIE, CF_4 gas was utilized to etch the area around the hardened PMMA bar. Following lift-off, a single set of contact leads was patterned on each channel region. Afterwards, the sample was loaded in the custom evaporator tool and the convergent ion source was operated at a beam energy of 600 eV (Fig. 1(b)) [14]. The recipe was started after the pressure in the chamber reached around 10^{-7} torr to ensure minimal contamination of the TMD etched edges. Immediately after the 15s etch, 15 – 25 nm of metal was deposited as the contact lead (Fig. 1(c)). These steps were repeated two more times to create two more sets of different metal leads on the same channel region. The three metals that were selected for WS_2 are Ag, Ti and Ni, while the ones for WSe_2 are Pd, Ti and Ni. The metals were selected based on their distinct work functions, observed reactivity to TMDs [27], and their performance in top-contacted devices. Fig. 1(d) depicts a completed device set with three different metal contacts on the same TMD film whereas Fig. 1(e) shows a cross-sectional transmission electron microscope (TEM) image of one device within that set.

For electrical testing, the devices were modulated by applying a back-gate voltage to the probe station stage (chuck), which is connected to the doped silicon substrate and gates the channel through the 300 nm SiO_2 gate oxide. All WS_2 transistors had channel length $L_{CH} = 200$ nm and channel width $W_{CH} = 3$ μm while the WSe_2 devices had $L_{CH} = 200$ nm and $W_{CH} = 4$ μm.

III. Results and Discussion

The Ti-WS_2 device surprisingly exhibited p-type conduction, as seen in the transfer characteristics in Fig. 2(a-b). This is unexpected considering the persistence of top-contacted WS_2 to form n-type or ambipolar transistors [28], [29], along with the Ti work function having close conceptual alignment with the charge neutrality level of WS_2, which is near the conduction band minimum (Fig. 2(c)). This interesting behavior was previously reported by researchers at imec as part of integrating WS_2 transistors in a 300 mm pilot line [25], [26]. The researchers contacted the edges of an embedded, atomic layer deposition (ALD) grown WS_2 channel using Ti/TiN side contacts [25]; however, they did not explore the underlying causes of the unexpected polarity shift. In our device, the sizable bandgap of WS_2 ($\sim$1.18 eV for a trilayer [30]) yielded a reasonable I_{ON}/I_{OFF} of $\sim 10^4$. The on-current of 0.16 μA/μm is modest and within the same order of magnitude as some edge-contacted MoS_2 demonstrations [16], [21], [22]. Unfortunately, the WS_2 sample had poor functional device yield of only 2-3 % with the analyzed Ti-WS_2 transistor in Fig. 2(a-c) exhibiting the top performance. This difference in yield compared to the imec work is attributed to our WS_2 being fully exposed to ambient conditions (i.e., no capping layers) whereas the imec devices had fully embedded WS_2 that was less prone to deleterious reactivity effects and mechanical deformation of the edge structure at the metal-semiconductor junction.

In addition to the WS_2 devices, three distinct metal contacts (Pd, Ti, and Ni) were explored on the same WSe_2 channel to eliminate performance differences due to film spatial variations. All three metal contacts performed quite similarly, with Pd having a slight edge with the best on-state, as seen in Fig. 2(d-e), including an on-current of 7.3 μA/μm. This on-current is comparable with some of the best values reported for edge-contacted MoS_2 [16], [21], [22], which is encouraging considering MoS_2 top-contacted FETs outperform their WSe_2 counterparts by a large margin. Moreover, the three WSe_2 devices had an impressive I_{ON}/I_{OFF} of $\sim 10^6$. The p-type behavior from the three metals is not as surprising as it was for Ti-WS_2 and it conforms with reported literature for top-contacted devices (conceptual band alignment illustrated in Fig.2(f)). The Ti-WSe_2 transistor did perform unexpectedly better than the Ni-WSe_2 device if the simple band alignment picture is used for comparison.

While the results we present for edge-contacted WS_2 and WSe_2 transistors are encouraging, top-contacted devices from the literature still outperform them [7], [31]. Top contacts have been heavily investigated for many years and have gone through numerous improvements and advancements. On the other hand, edge contacts (particularly to W-based TMDs) have not reached the same level of maturity to justify a direct comparison. Extensive research is still required to demystify the carrier injection behavior at edge interfaces and optimize the fabrication approach. Theoretical studies have suggested better performance from edge contacts than their top contact counterpart [18], but more extensive experimental studies are needed to validate this projection.

Cross-sectional TEM imaging was conducted on the electrically characterized devices to confirm edge contact formation as depicted in Fig. 3(a-b). The TEM images, along with energy dispersive spectroscopy (EDS) analysis, revealed intriguing insight beyond edge contact verification. Fig. 3(c-d) reveals the existence of a W layer beneath the metal contact, which originates from the etched WSe_2 in spite of substrate over-etching. The lack of this effect in edge-contacted MoS_2 transistors could be due to W being twice as heavy as Mo, leading it to settle into the etched substrate rather than be fully evacuated from the contact region. Se (or S for WS_2) was also present below the contact (Fig. 3(c)), albeit with a less-prominent signal than W. It is important to note that WS_2 devices, such as the one in Fig. 3(a), also exhibited the same W-residual effect. These findings can explain why three metal contact materials displayed similar I-V curves for WSe_2 as the transistor effectively utilized W, or a compound therefrom, as the edge-contact material. The device yield discrepancy between WS_2 and WSe_2 samples could also be explained by the high resistivity of residual S beneath WS_2 contacts compared to the more conductive Se below WSe_2 contacts.

Based on the EDS data, the most likely explanation for the p-branch-dominant behavior of the Ti-WS_2 device is that a composite metal was formed and serves as the contact rather than pure Ti or W. This is not to suggest that it is simply metal work function modification from such a metal compound that is responsible for the polarity shift; modification of the work function would be only one factor along with the change

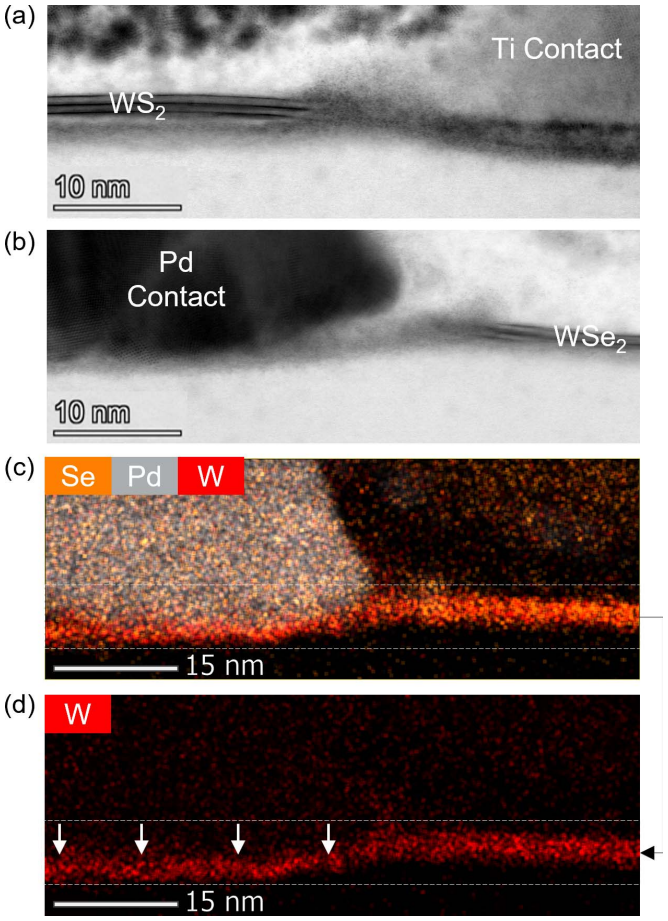

Fig. 3. Cross-sectional TEM images of the fabricated edge-contact devices. (a) TEM image of Ti-WS_2 device confirming edge contact formation on the trilayer WS_2. (b) TEM image of Pd-WSe_2 device confirming edge contact formation on the bilayer WSe_2. (c) EDS elemental map of Pd-WSe_2 device only highlighting Pd, Se and W. (d) EDS elemental map of image in (c) only highlighting W, showing significant W content beneath the contact region despite over-etching of the substrate.

in bonding structure, pinning behavior, and various carrier transport dynamics. Other potential factors contributing to this phenomenon are the apparent damage to the WS_2 channel near the metal contact (Fig. 3(a-b)), though the devices from Ref. [25] did not appear to present this interfacial damage and still exhibited unexpected p-type behavior. Ultimately, this observation of residual W and chalcogen in edge contacts makes it possible for further, more focused analyses to be carried out towards understanding these distinct interfaces.

IV. Conclusion

We presented the creation of edge-contacted transistors on less-investigated TMDs, namely, WSe_2 and WS_2. A convergent Ar^+ ion beam source that is embedded in a custom, high-vacuum e-beam evaporation chamber is utilized for *in-situ* processing. The Ti-WS_2 device exhibited unanticipated p-type conduction whereas three metals (Pd, Ni and Ti) performed similarly on WSe_2. TEM imaging and EDS analysis unraveled some of the mystery by indicating the presence of a residual W-Se (for WSe_2 FETs) or W-S (for WS_2 FETs) layer beneath the metal contacts despite the over-etched substrate. Consideration of this unique etching effect could be essential for tungsten-based, edge-contacted TMD transistors.

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